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FSiC2022

Free Silicon Conference

65nm CMOS Design-Flows on Free and Open-Source Tools : An Overview

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- ➢ Design-kits Distribution.
- ➢ Technical support.
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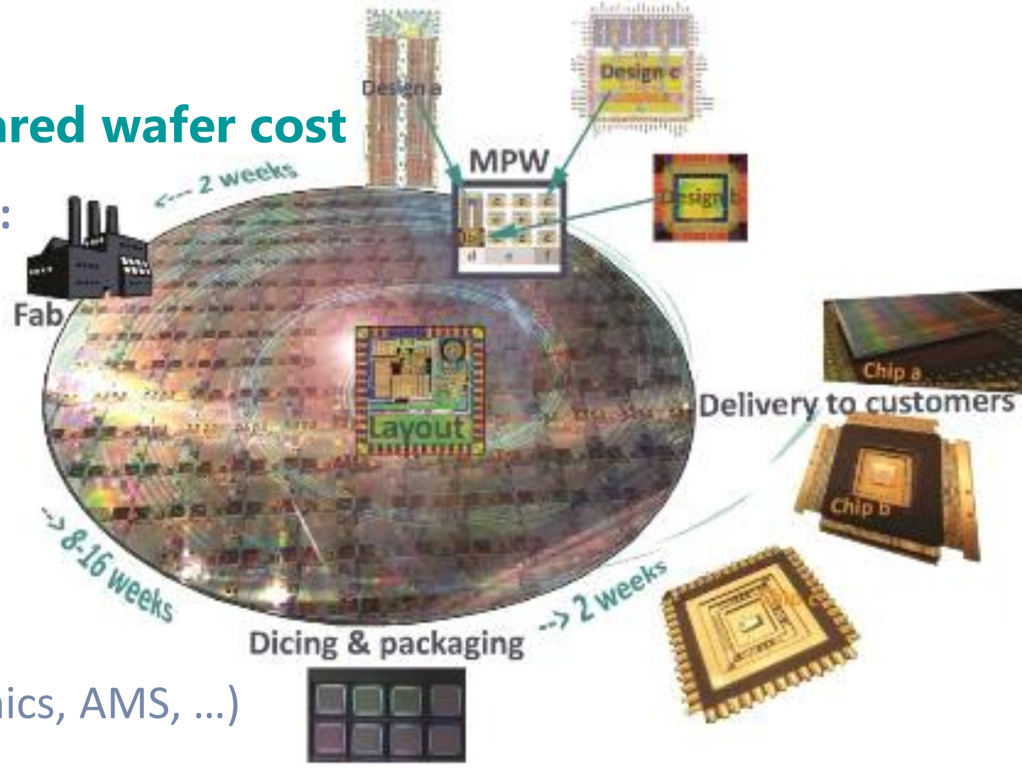
- ➢ Designs clustering / Reticle.
- ➢ Fabrication at Foundries (STMicroelectronics, AMS, …)
- ➢ Additional services (dicing, thinning, packaging, …)
- ➢ Circuits Delivery to customers.



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Summary

- Introduction

- Full-custom PDK & Design-Flow on a 65nm CMOS :
  - Techfiles, devices symbols and P-cells.
  - Custom GUI for Spice and waveform viewer

- RTL-to-GDS Digital Design-Flow in a 65nm CMOS :
  - Techfiles, standard-cell libraries.
  - Custom scripts and GUI interface

- Demos of the 2 design-flows

- Conclusion

Introduction

□ **Today, Free and Open-source CAD tools are gaining performance, compliance to standard EDA formats, better support for scripting and GUI, then allowing more interoperability.**

□ **Very few Silicon Foundries are exploring seriously open-source CAD tools (e.g. the Google/SkyWater initiative for open PDK 130nm CMOS).**

□ **Free and open-source CAD tools used in this work :**

- **Glade**: IC layout / schematic editor (reading and writing common EDA formats), with DRC, LVS, PEX.
- **NGspice**: Spice simulator
- **Gaw**: Analog waveform viewer
- **Icarus Verilog**: Verilog simulator
- **GTKwaves** : Digital waveform viewer
- **YOSYS** : Logic Synthesis
- **OpenROAD** : Automatic Place & Route Framework : (ICeWall, ioPlacer, iFP, Tapcell, PDNGEN, RePlAce, OpenDP, TritonCTS, FastRoute, TritonRoute, OpenRCX, OpenSTA, and more …)
- **KLayout** : Viewer and Editor

□ **Goal : Define consistent design-flows running free & open-source tool-chains with a Foundry PDK & std-cells libraries.**

Full-Custom Design-Flow

65nm Full-Custom Design Flow

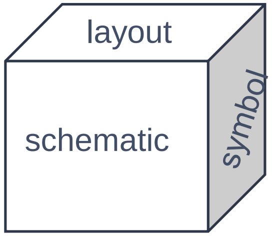
❑ Front-end CAD Tools :

- Schematic entry / Spice simulation / Waveform :

Glade http://www.peardrop.co.uk

Ngspice https://ngspice.sourceforge.io

GAW https://gaw.tuxfamily.org



❖ Unified cellview concept :

➢ layout, schematic, symbol, netlist, extracted

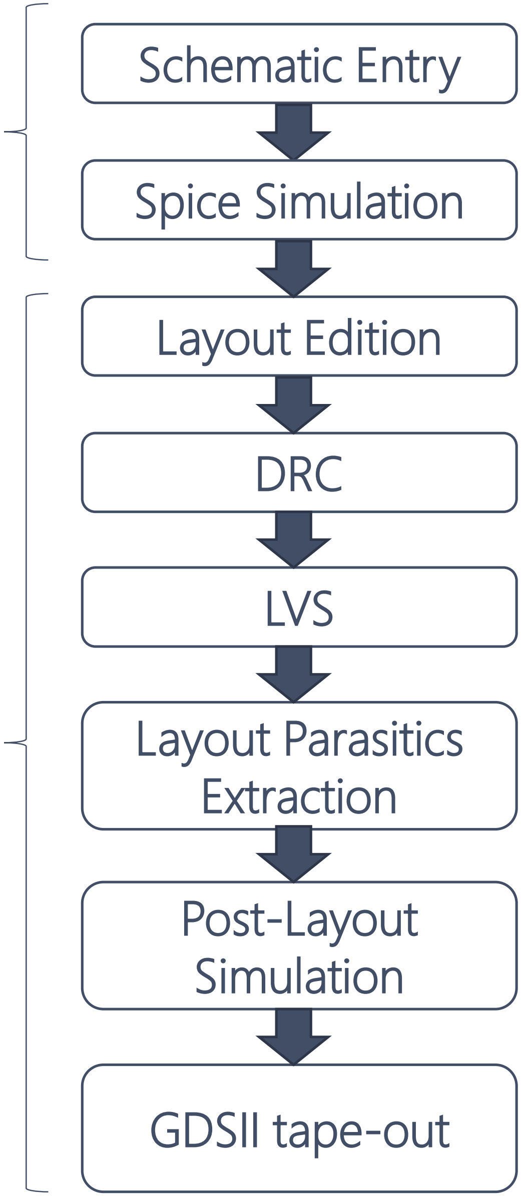
❑ Backend CAD Tools :

- SDL / Layout / DRC / LVS / PEX :

Glade http://www.peardrop.co.uk

Gemini : (embedded in Glade)
https://www.cs.washington.edu/research/gemini-netlist-comparison-project

Ngspice + GAW for Post-layout Simulation



65nm Full-Custom Design Flow (front-end)

❑ Front-end CAD Flow :

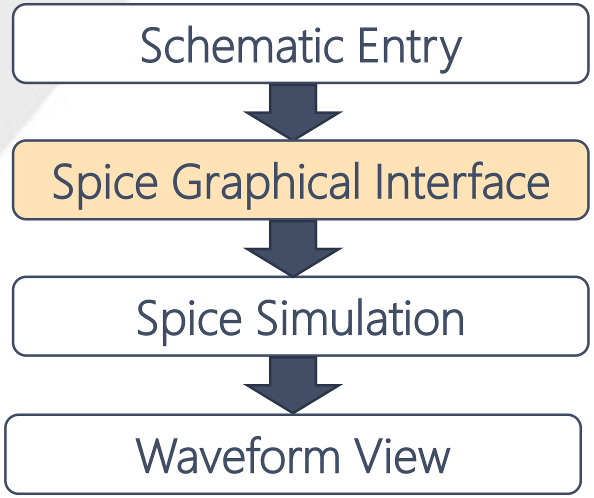
- Schematic entry / Spice simulation tools
  Waveform viewer :

Glade http://www.peardrop.co.uk

Spice GUI (TCL/TK custom development)

Ngspice https://ngspice.sourceforge.io

GAW https://gaw.tuxfamily.org

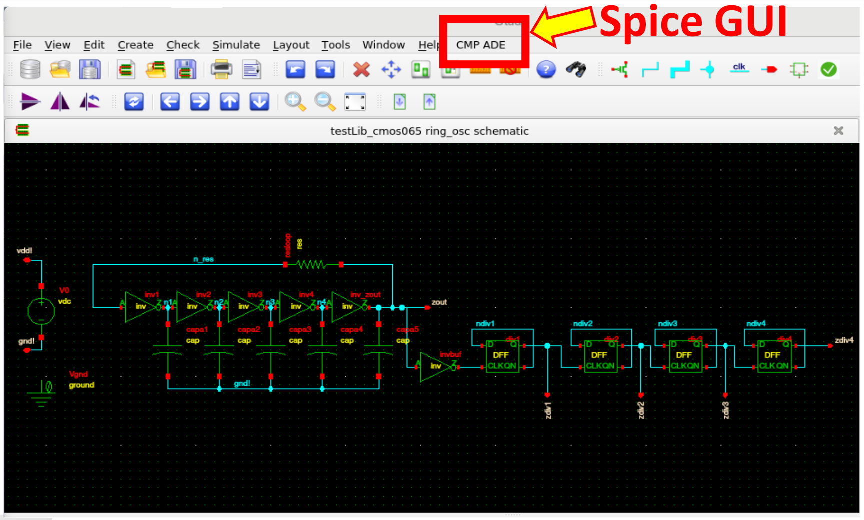


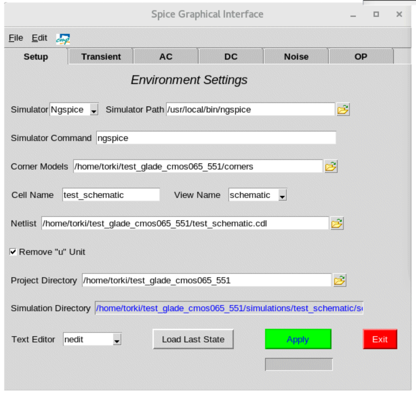
Schematic Entry

Spice Graphical Interface

Spice Simulation

Waveform View





Spice Graphical Interface

File Edit

Setup | Transient | AC | DC | Noise | OP

Environment Settings

Simulator Ngspice Simulator Path /usr/local/bin/ngspice

Simulator Command ngspice

Corner Models /home/torki/test_glade_cmos065_551/corners

Cell Name test_schematic View Name schematic

Netlist /home/torki/test_glade_cmos065_551/test_schematic.cdl

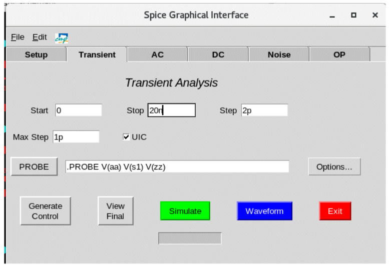
☑ Remove "u" Unit

Project Directory /home/torki/test_glade_cmos065_551

Simulation Directory /home/torki/test_glade_cmos065_551/simulations/test_schematic/s

Text Editor nedit

Load Last State | Apply | Exit



Spice Graphical Interface

File Edit

Setup | Transient | AC | DC | Noise | OP

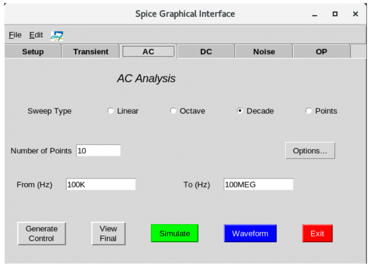
Transient Analysis

Start 0 Stop 20n Step 2p

Max Step 1p ☑ UIC

PROBE .PROBE V(aa) V(s1) V(zz) Options...

Generate Control | View Final | Simulate | Waveform | Exit



Spice Graphical Interface

File Edit

Setup | Transient | AC | DC | Noise | OP

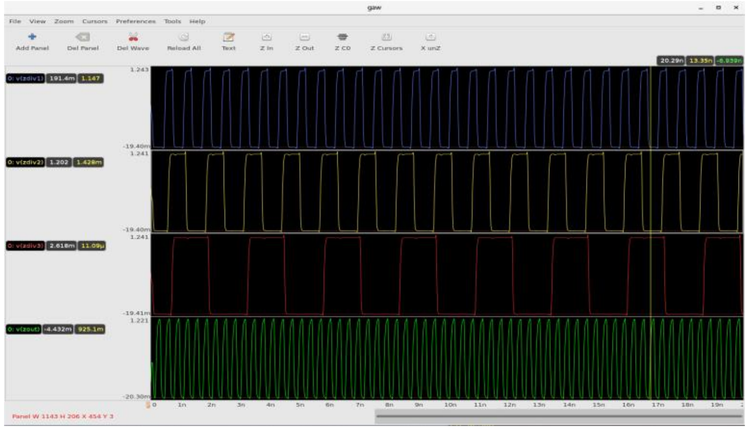
AC Analysis

Sweep Type ○ Linear ○ Octave ● Decade ○ Points

Number of Points 10 Options...

From (Hz) 100K To (Hz) 100MEG

Generate Control | View Final | Simulate | Waveform | Exit

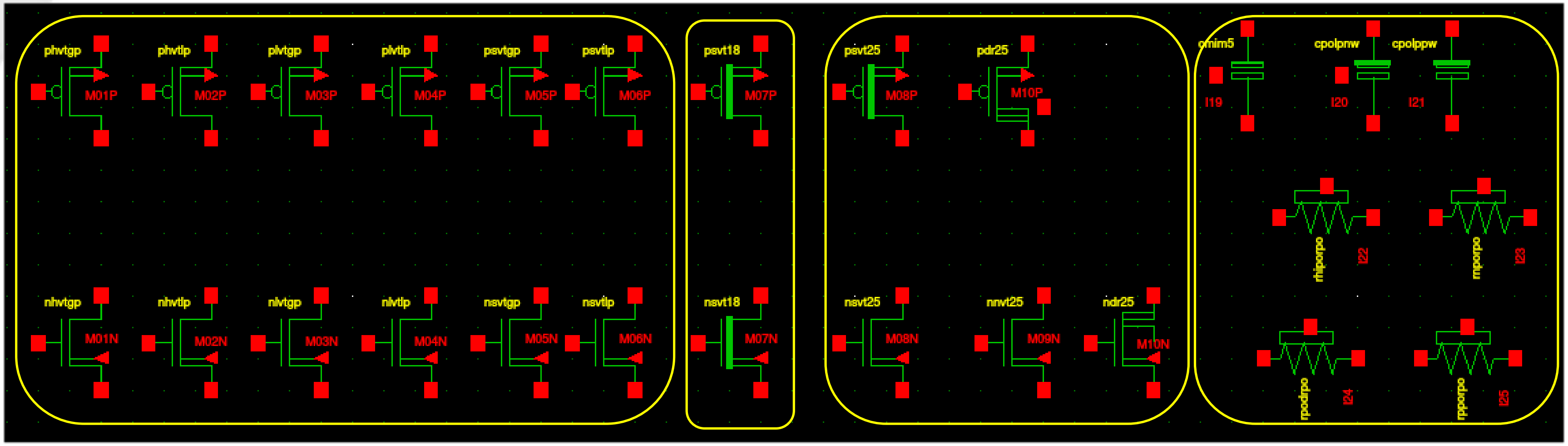


65nm Full-Custom Design Flow (front-end)

❑ Front-end PDK :

- Schematic entry : 27 Device symbols (MOS, capacitors, resistors)
- **Spice Graphical Interface** : 1’500+ lines in TCL/TK compiled using **freewrap** : https://sourceforge.net/projects/freewrap
- Spice simulation : Foundry MOS models are BSIM4v5 Spice models fully supported by **Ngspice**. RAW format is generated for waveforms.
- Waveform viewer : **GAW** for waveforms display (RAW format).

1.2V MOSes 1.8V 2.5V MOSes Capacitors Resistors



65nm Full-Custom Design Flow (backend)

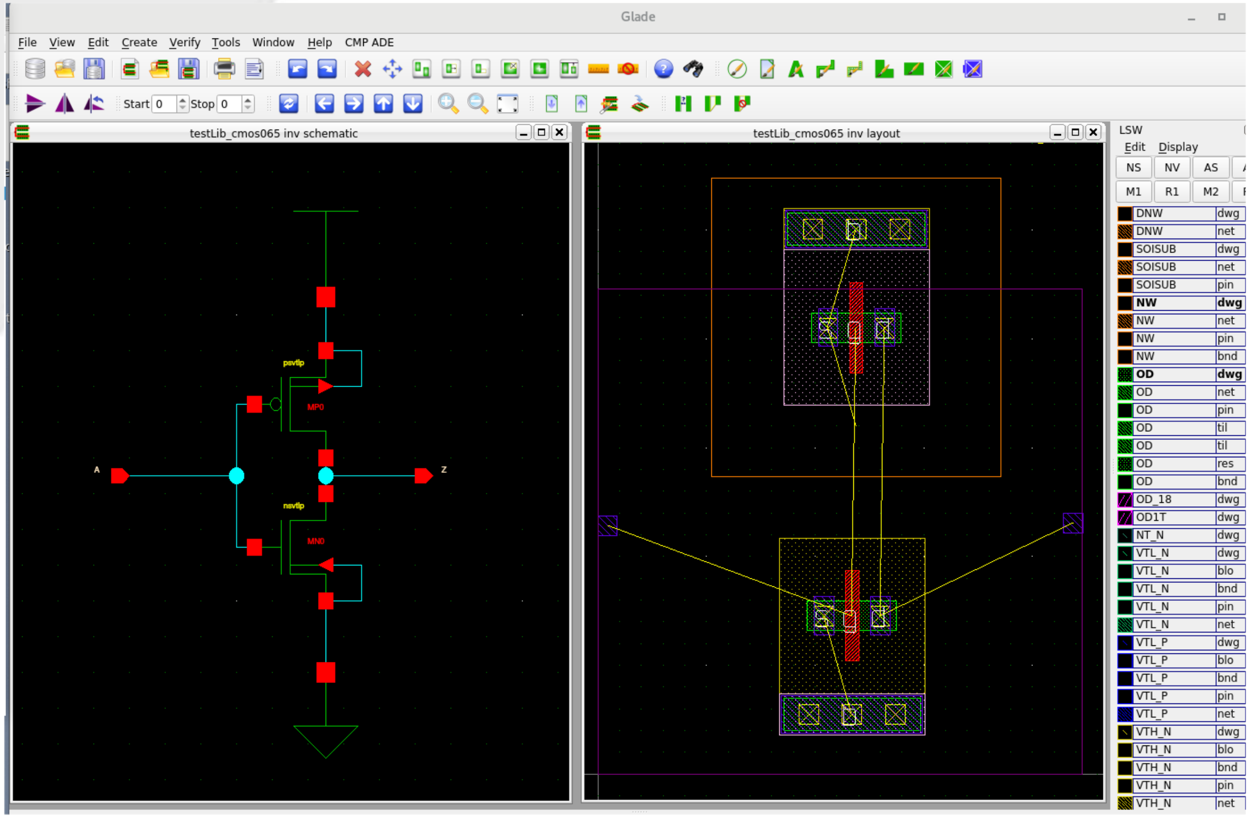
❑ Backend CAD Tools :

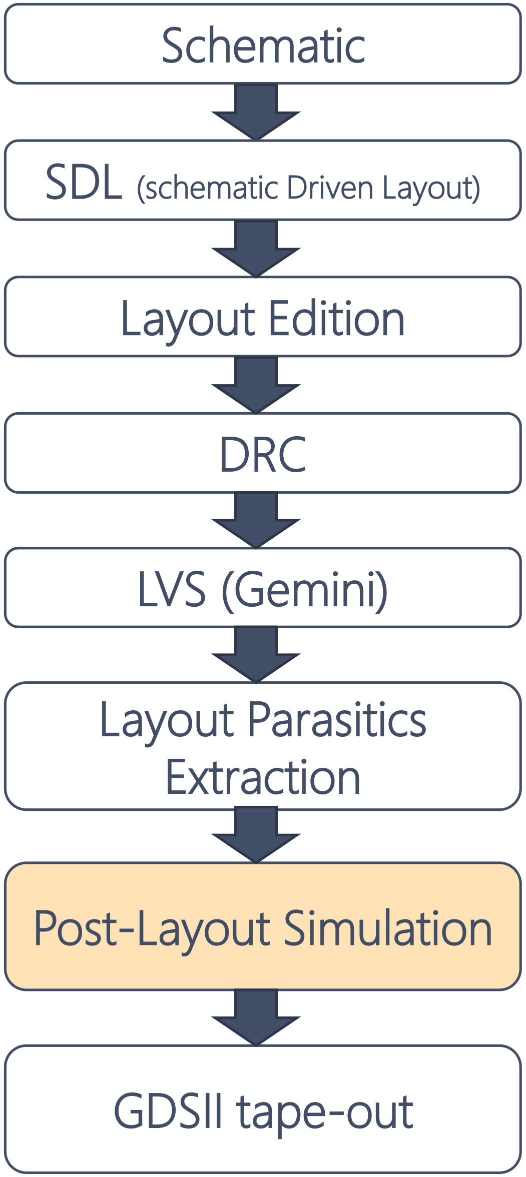
- Layout Editor with SDL / DRC / LVS / PEX:

Glade http://www.peardrop.co.uk

Gemini : (integrated to Glade)

https://www.cs.washington.edu/research/gemini-netlist-comparison-project





Schematic

SDL (schematic Driven Layout)

Layout Edition

DRC

LVS (Gemini)

Layout Parasitics Extraction

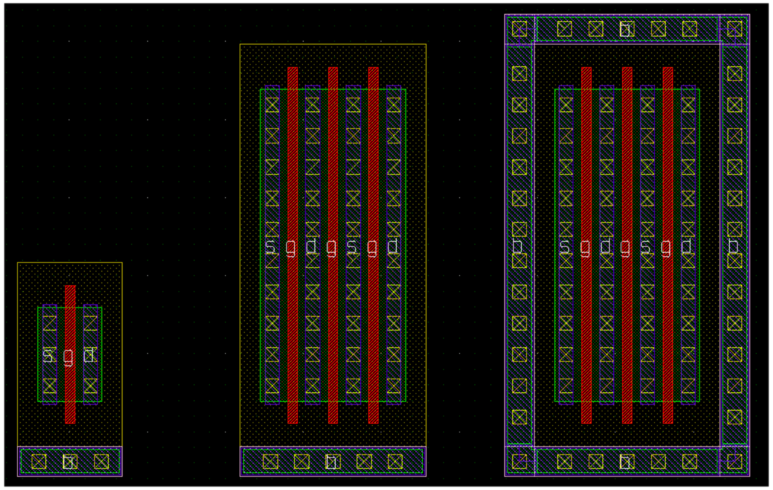
Post-Layout Simulation

GDSII tape-out

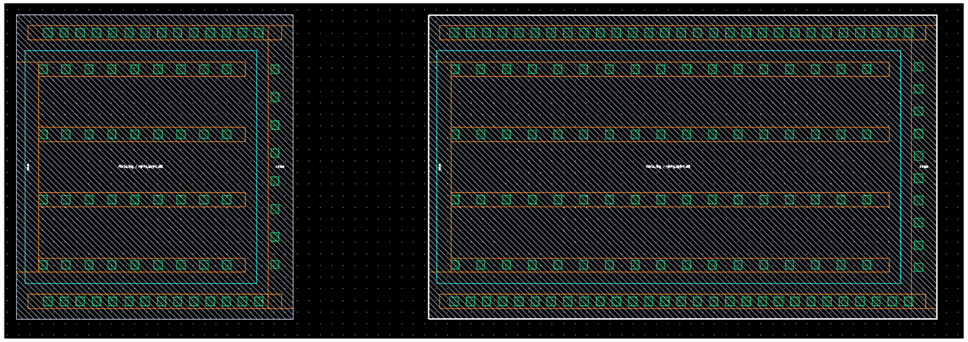
65nm Full-Custom Design Flow (backend)

❑ Primitive devices available as Pcells : MOS, Capacitors, Resistors

- Pcells are written in Python (compiled with Cython)
- MOS is in the range of 250-500 lines code per cell.
- About 11k lines written for all primitive devices.



- MOSes features :
  - Multi-fingers,
  - Parametrized guardring & Taps.



- MiM capacitors features :
  - Callbacks between W & L and C
  - 100% balanced Vias count on plates (no antenna rules violation)

Video Demo Spice Simulation

Video Demo Spice Simulation

Full-Custom Design-Flow

RTL to GDS Digital Design-Flow

65nm Digital Design Flow RTL to GDS

❑ Front-end CAD Tools :

- RTL simulation / Waveform / Logic Synthesis:

Icarus Verilog http://iverilog.icarus.com

GTKWave http://gtkwave.sourceforge.net

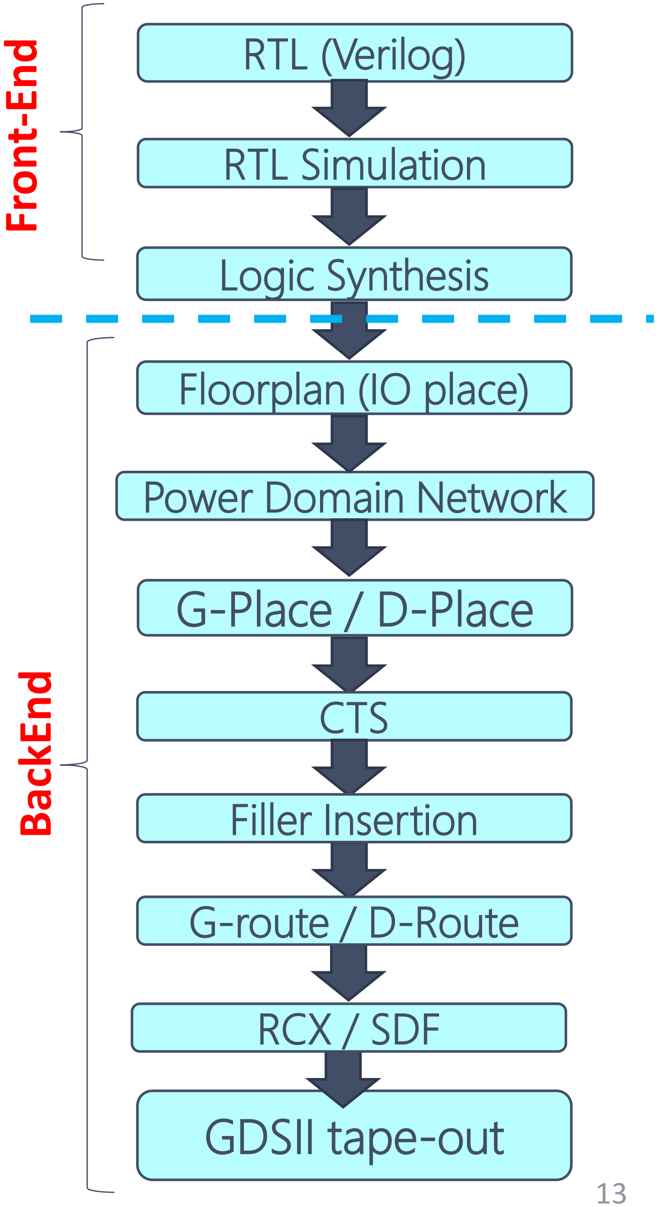
YOSYS https://yosyshq.net/yosys

❑ Backend CAD Tools :

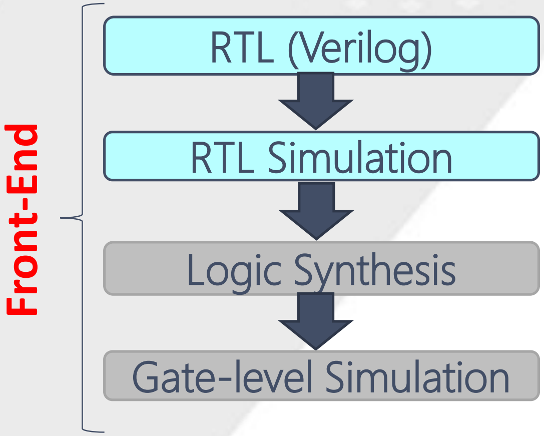
- Floorplan / P&R / CTS / RCX / GDSII Layout :

OpenROAD : Automatic Place & Route Framework : (ICeWall, ioPlacer, iFP, Tapcell, PDNGEN, RePlAce, OpenDP, TritonCTS, FastRoute, TritonRoute, OpenRCX, OpenSTA, and more …) https://theopenroadproject.org

KLayout https://www.klayout.de



Digital Design-Flow (Front-end)

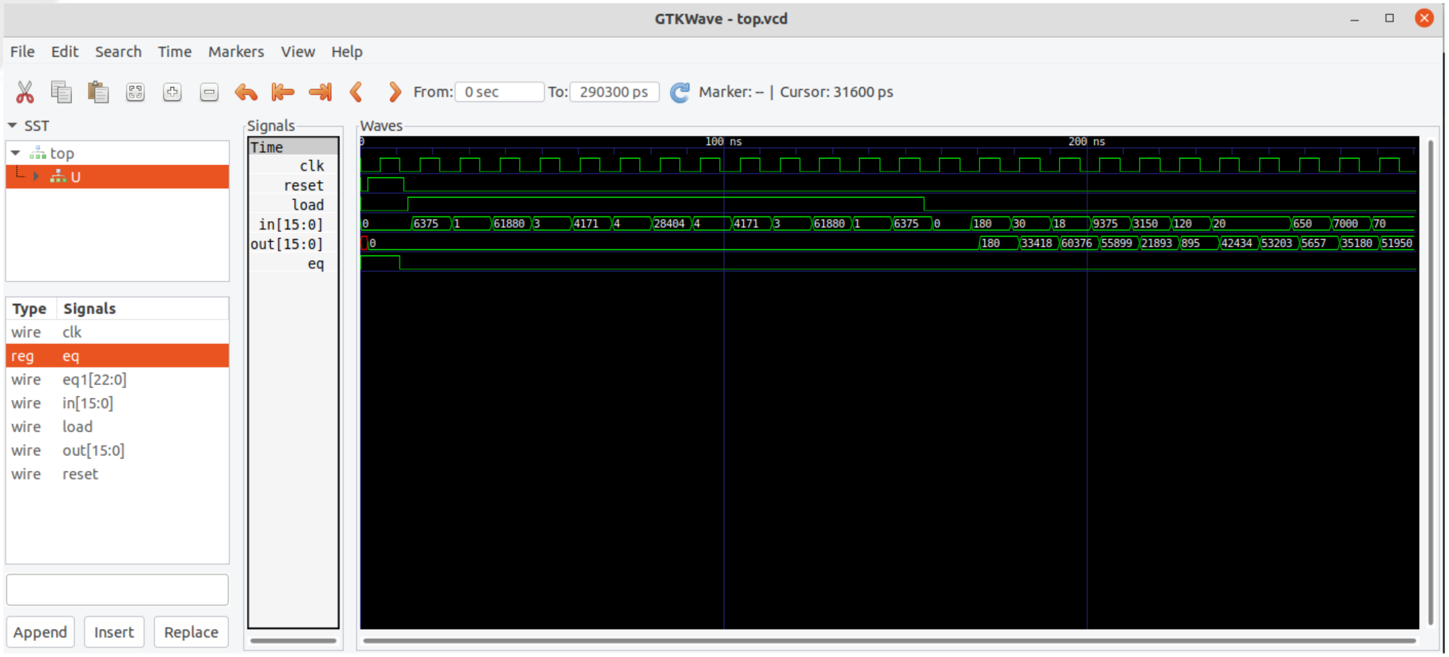


❑ Verilog RTL Simulation:

- RTL code + Testbench

iverilog => vpp => VCD file (Value Change Dump)

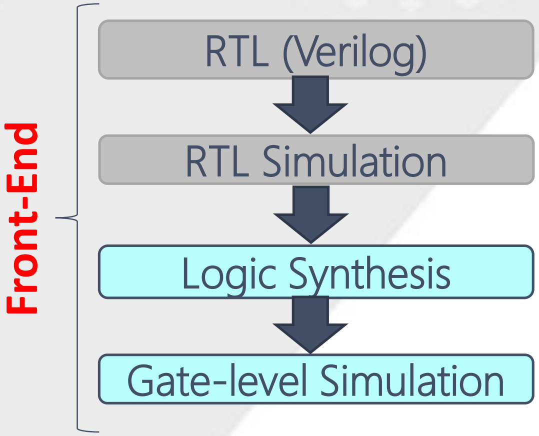
VCD file => GTKWave


GTKWave - top.vcd

From: 0 sec To: 290300 ps Marker: -- | Cursor: 31600 ps

Type	Signals
wire	clk
reg	eq
wire	eq1[22:0]
wire	in[15:0]
wire	load
wire	out[15:0]
wire	reset

Digital Design-Flow (Front-end)



Front-End

RTL (Verilog)

RTL Simulation

Logic Synthesis

Gate-level Simulation

❑ Verilog Synthesis:

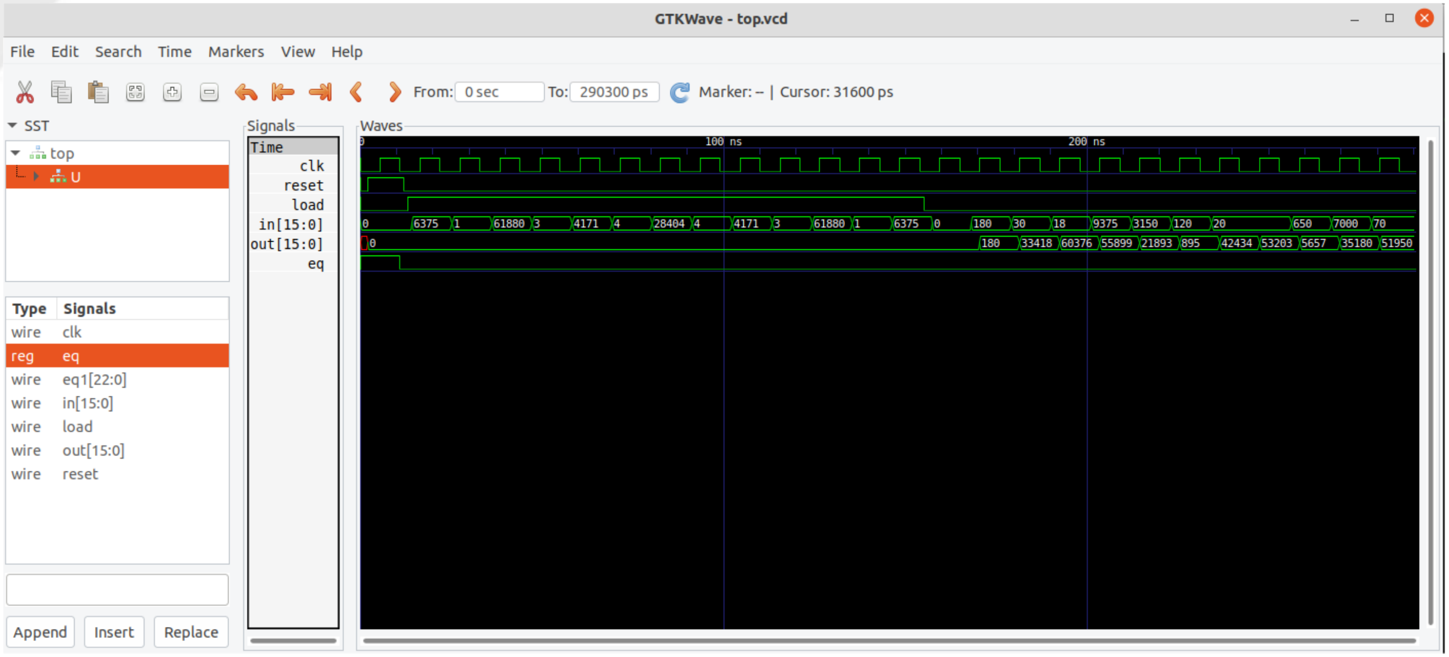
- RTL code + SDC file (constraints) + std-cells Liberty (.lib)

Yosys / ABC => Verilog Gate-level Netlist

- Verilog Netlist + Testbench + Verilog std-cells library

iverilog => vpp => VCD file (Value Change Dump)

VCD file => GTKWave

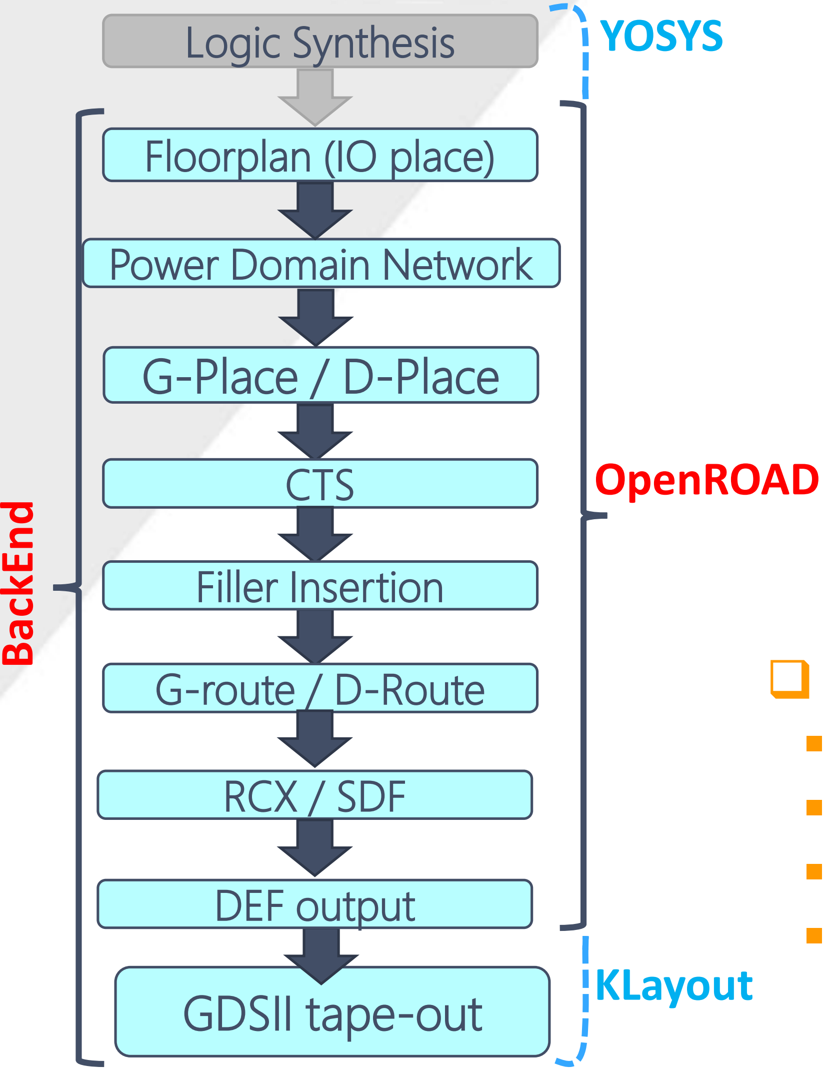


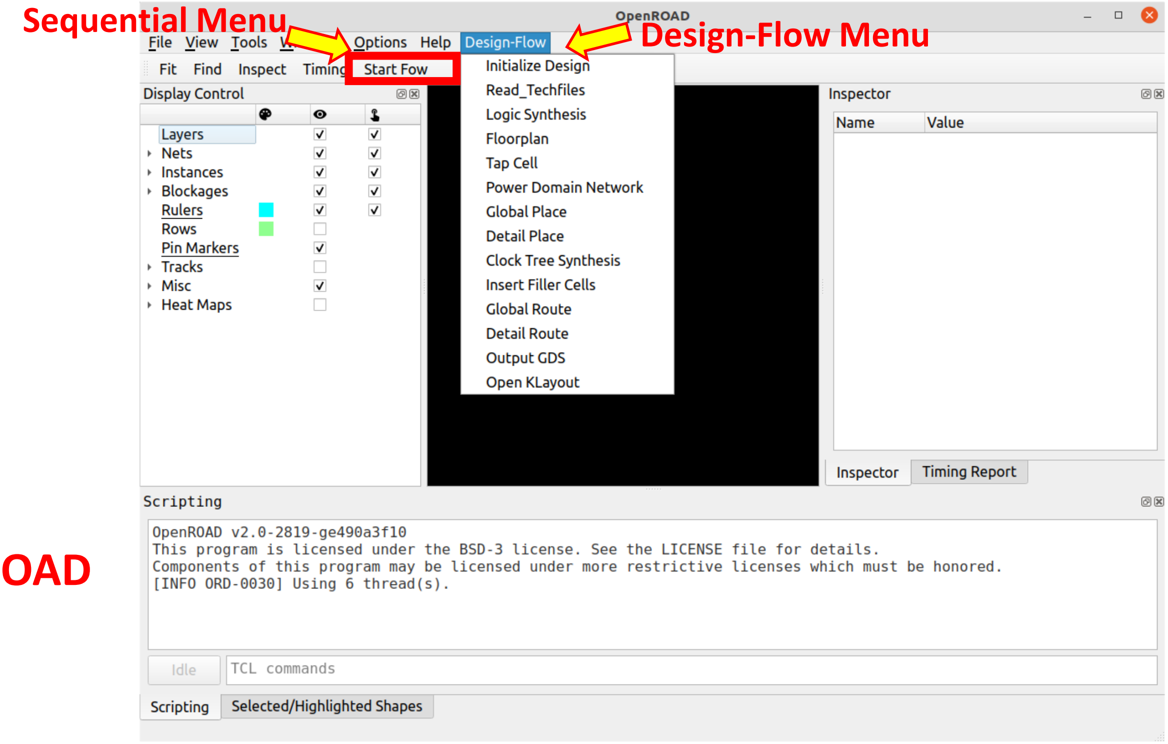
GTKWave - top.vcd

From: 0 sec To: 290300 ps Marker: -- | Cursor: 31600 ps

Type	Signals
wire	clk
reg	eq
wire	eq1[22:0]
wire	in[15:0]
wire	load
wire	out[15:0]
wire	reset

Digital Design-Flow (Backend)





```
OpenROAD v2.0-2819-ge490a3f10
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
[INFO ORD-0030] Using 6 thread(s).
```

❑ Automatic Place & Route:

- OpenROAD is a toolchain Framework.
- YOSYS added at front.
- Klayout added at end.
- Custimized TCL/TK scripts (600 lines) easily running with any design adding to the GUI :
  - ✓ Scrolling menu
  - ✓ Sequential buttons menu

Video Demo RTL to GDS

Video Demo RTL to GDS

Conclusion & Perspectives

□ **Complete full-custom design-flow with tools-chaining & integrated environment on a 65nm CMOS**.

□ **Complete Digital design-flow from RTL to GDS on a 65nm CMOS technology.**

□ **Reference Foundry’s PDK has been used** *almost as is* **to ensure the free and open-source EDA tools running consistently through the reference flows.**

□ **Need a deep discussion with Foundries how to make these development available to the community and explore the common interest.**

□ **Still some issues to be solved :**

✓ **DRC rules are implemented with a coverage of 85%. Some specific DRC rules are not implemented.**

✓ **Same for analog parasitic extraction : the performance and accuracy of the 2.5D is not meeting the Foundry’s reference tools (sign-off tools).**

✓ **SDF back-annotation not working with Icarus Verilog (?)**