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German Microelectronics Design Initiative
Federal Ministry of Education and Research (BMBF)

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(VDI/VDE Innovation + Technik GmbH)

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BMBF focus topic: chip design

- Strengthening research, development and innovation in the core area of chip design
- Driving innovations in the development of chips and systems
- Establishing and expanding the chip design ecosystem in Germany
- Close integration with the EU Chips Act

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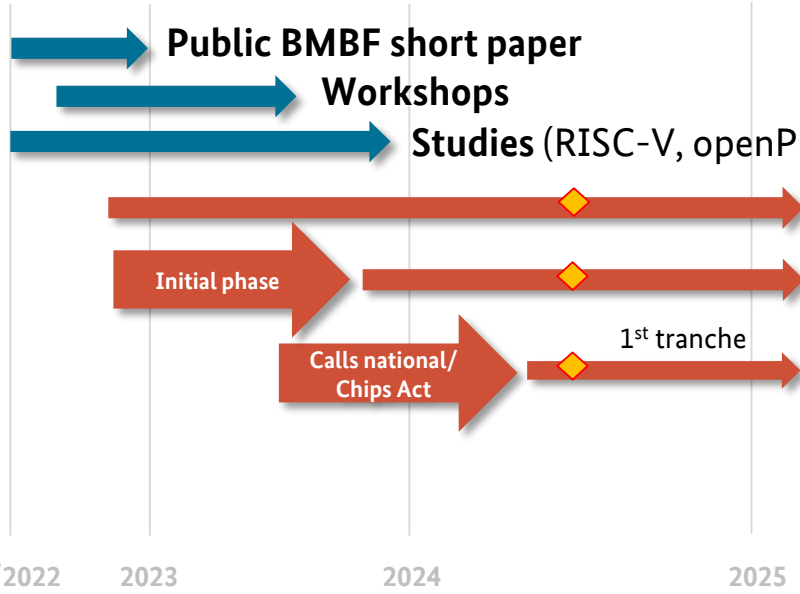
Implementation



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Funding program „Design Instruments for Sovereign Chip Development with Open Source (DE:Sign)“

bmbf.de

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DE:Sign | Overview

- Design tools, methods and chip designs **focussed on open source**
- Significant development of the tool chain
- Participation of young academics and talents
- Close collaboration with „ChipDesign Germany“
- Industry- or science-driven, pre-competitive joint or individual R&D projects
- Universities, research institutions, companies

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DE:Sign | Research focus

a. Open source **EDA tools**, PDKs und IP libraries

b. Open source **design methods**

c. Novel **chip designs** based on open source EDA tools, PDKs, and IP

d. Design tools, PDKs and IP for **novel technologies**

(e.g. chiplets, advanced packaging, MEMS, radio frequency)

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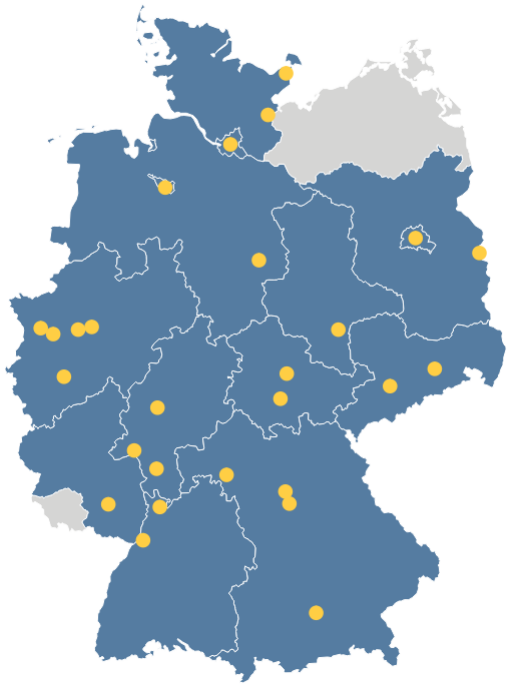
DE:Sign | Key figures

- **Deadline**: 31 July 2023
- **Submissions:** 36 pre-proposals
  with 150 partners (in total)
- **Selection meeting:** 29 September 2023
- **Selection:** 15 R&D projects with 62 partners (in total)
  (thereof 12 industrial partners)
- 11 joint projects, 4 individual projects
- **Grant (total):** 29.6 Mio. EUR



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DE:Sign | R&D projects open source EDA tools

Talents: Student competition „Open source chip design challenge“ (**OCDCpro**)

Analog design

- ✓ Text based design (**ORDeC**)
- ✓ High frequency chips (**DEMICO**)

Digital design

- ✓ eFPGAs (**OWAS**)
- ✓ FPGAs (**FEntWumS**)
- ✓ RISC-V (**GATE-V**)
- ✓ Verification (**OSVISE**)
- ✓ DRAM (**DERAMSys**)
- ✓ AI hardware (**EDAI**)

Hardware security

- ✓ HW architecture (**ExViPaS**)
- ✓ HW security module (**SIGN-HEP**)

Novel technologies

- ✓ RFETs (**ReDesign**)
- ✓ MEMS/ASIC (**Meta-X**)
- ✓ Packaging/SiP (**PASSIONATE**)
- ✓ Radiation hardened HW (**Flowspace**)

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DE:Sign | Open source ecosystem

EDA area	OSVISE	OCDCpro	OWAS	DEMICO	Meta-X	ExViPaS	Flowspace	EDAI	ReDesign	GATE-V	PASSIONATE	FEntwumS	DERAMSys	ORDeC	SIGN-HEP	Σ
PDK and IP		x	x	x	x		x	x	x	x			x	x		**10**
Standard cells, libraries, IP		x	x	x	x		x	x	x	x			x	x		10
Simulation models		x		x	x		x		x				x			6
System design	x	x	x	x	x	x	x	x		x	x	x	x	x	x	**14**
System specification		x	x	x	x	x		x			x	x		x		9
Architecture						x	x	x		x	x			x	x	7
Design flow	x	x	x	x	x		x	x		x		x	x	x	x	12
Digital design	x	x	x		x	x		x	x	x		x	x		x	**11**
HDL/Logic design	x	x	x		x	x				x					x	7
Logic simulation/-verification	x	x	x		x	x						x	x		x	8
Circuit synthesis	x	x	x		x			x	x	x		x	x		x	10
Analog design/Full custom				x	x		x	x	x				x	x		**7**
Circuit synthesis				x	x				x				x	x		5
Analog simulation/-verification				x			x	x	x				x	x		6
Novel and specific substrates					x		x		x							3
Layout		x	x	x	x		x	x	x		x			x	x	**10**
Layout design		x		x	x		x				x			x		6
Layout synthesis		x	x		x		x	x	x					x	x	8
Layout verification		x		x	x										x	4
LVS/PEX/...		x		x	x										x	4
Production		x	x	x	x		x		x		x				x	**8**
Tape out		x	x	x	x		x		x		x				x	8
Packaging											x					1
Test			x	x					x							3

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DE:Sign | Open source ecosystem

EDA area	OSVISE	OCDCpro	OWAS	DEMICO	Meta-X	ExViPaS	Flowspace	EDAI	ReDesign	GATE-V	PASSIONATE	FEntwumS	DERAMSys	ORDeC	SIGN-HEP	Σ
PDK and IP		x	x	x	x		x	x	x	x			x	x		**10**
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Circuit synthesis	x	x	x		x			x	x	x		x	x		x	10
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Layout		x	x	x	x		x	x	x		x			x	x	**10**
Layout creation		x		x	x		x				x			x		6
Layout synthesis		x	x		x		x	x	x					x	x	8
Layout verification		x		x	x										x	4
LVS/PEX/...		x		x	x										x	4
Production		x	x	x	x		x		x		x				x	**8**
Tape out		x	x	x	x		x		x		x				x	8
Packaging											x					1
Test			x	x					x							3

Why another ecosystem?
Why open source?

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“Open source tools are cute and nice for education but utterly useless in industry. Shifting away from professional tools is foolish."

"We cannot earn money with open source”

“Open source provides neither support, nor liability.”

“Funding open source EDA will only benefit China”

“The commercial tools are extremely sophisticated and advanced. It's pointless to try catching up, esp. with open-source. ”

“Open-source projects threaten and destroy business models“

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“Open source provides neither support, nor liability.”

→ Support for open source projects is often outstanding (Stack Overflow, Discord, the Linux communities, …)
→ Proprietary tools emerge and go down with their businesses (liability & support can be lost instantly and unpredictably)
→ So do their features, default settings, usage conditions, price options, etc.
→ Liability conditions in EDA are considered particularly problematic (recent survey for the EU Design Platform)

Conclusions:
Support for open source projects is often better than for commercial tools.
Liability might be as well.

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“Open source tools are cute and nice for education but utterly useless in industry. Prioritizing open source EDA is dangerous and foolish." – Industry

→ Priority is on the proprietary tool chain.
→ Past priorities have led to the current state of the EDA.
→ Also industry: *“Labor shortage, labor shortage! Young talents are missing! ~~We~~ The government needs to make chip design more attractive!”*
→ Precondition for public R&D funding: The associated (financial) risks need to be so high that the company cannot conduct the project without aid.

“The commercial tools are extremely sophisticated and advanced. It's pointless to try catching up, esp. with open-source.”

→ Essential components of the commercial tool chain were once university projects.
→ The tools consist of code, no magic involved (pun intended).
→ The more wheels exist, the easier it becomes to invent new ones.
→ Not advanced: No browser interfaces, no Python libraries, no CI/CD platforms, no AI/ML interfaces, etc.
→ Commercial EDA tools rarely hang out with modern software technology

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“Funding open source EDA will only benefit China”

→ China is developing its own EDA ecosystem (many parts of it seem to be open source)
→ Likely cheaper, more accessible, modern, flexible, and interoperable.
→ Better access and usage conditions will attract new users and chip designers.
→ Permissive licenses + large community will likely lead to shared development efforts, reusable designs, and increased development efficiency (e.g. open, versioned IP pool).

Conclusion:
Not reforming our current tool chain will almost certainly benefit China.

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DE:Sign | Reasons for open source EDA

- Intrinsically free and accessible
- Flexible, extensible, and interoperable through open standards, interfaces, and file formats
- Open source code provides transparency, trustworthiness, and security
- Shared development is less development for every company and individual
- Popular among young people
- Sustainably protected from acquisitions
  (commercial EDA projects have received funding for decades)
- ...

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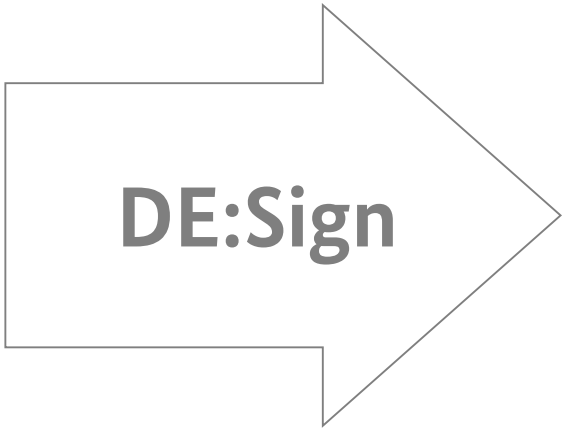
DE:Sign | Goals

EDA (now)

- **Expensive** and **risky**
- **Complicated** and **opaque**
- **Outdated** and **non-welcoming** user interfaces
- **Closed** application interfaces and poor interoperability
- **Ageing** and **distanced** community
- **Oligopoly** market



EDA (future)

- **Fairly priced** and **reliable**
- **Transparent** and **trustworthy**
- **Modern** and **pleasant** user interfaces
- Modern and **open** application interfaces
- **Young** and **welcoming** community
- **Diverse** market

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German Microelectronics Design Initiative of the Federal Ministry of Education and Research (BMBF): Further components

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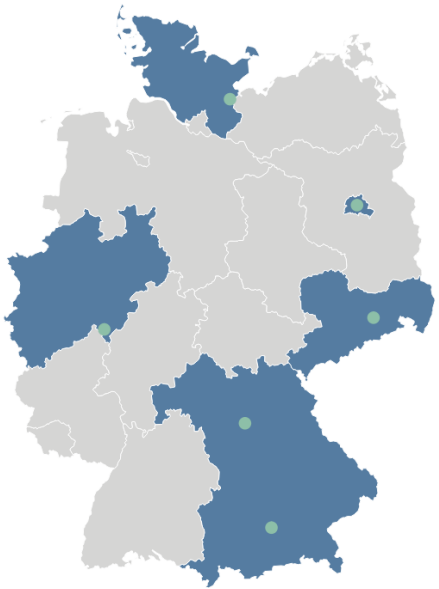
DE-TW | R&D collaboration with Taiwan

- **Deadline:** 31 July 2023 (letter of interest)
- **Deadline:** 5 September 2023
- **Submissions:** 8 pre-proposals with 17 partners (in total)
- **Selection meeting:** 4 October 2023, 15 March 2024
- **Selection:** 6 projects with 12 partners (in total)
- 1 German partner in each joint project
  (universities, research institutions)
- **Grant (total) (DE):** 3.3 Mio. EUR



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DE-TW | R&D projects with Taiwan

Talents: at least 1 student exchange per student and project, in all 6 projects

RF electronics

- ✓ Chips for high frequencies (110 bis 170 GHz) (**ATTRACTS**)

International collaboration

- ✓ Strong interaction and networking
- ✓ Effective integration of individual research

Edge AI electronics

- ✓ Photonic chips for high speeds (**PNN**)
- ✓ Compute-in-memory modules (**FeEdge**)
- ✓ Memristive chips in biosensing (**NeuroMemSense**)
- ✓ Open source EDA tools/design methods for secure AI accelerators (**TEdgeAI**)
- ✓ Open source simulator for photonic interconnects in 3D chip systems (**PI3D**)

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CHIP DESIGN GERMANY

Chipdesign Germany

- **Start:** 1 November 2023
- Central contact point for pre-competitve exchange of all players from research, science and industry in the field of chip design in Germany
- Initiation of working groups on specific topics, including open source EDA tools
- Collecting/accessing all results of open source design tools of BMBF funding program “DE:Sign”
- University alliance and Microelectronics Academy (FMD) support education/training of talents
- **Grant (total):** 3.8 Mio. EUR
- **Funding period:** 3 years, then self-sustaining

https://www.chipdesign-germany.de

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Open source design tools for sovereign chip design – research study on status and perspectives

- Topics: **TRL, business perspectives, innovation mechanisms, compliancy with industry demands**
- Focus: **analog**, **RF**, digital & mixed-signal, novel devices (e.g. MEMS, SiP)
- Tight collaboration with **Chipdesign Germany** & **Industry Networks** (e.g. VDMA, VDA, BDSV)
- 01.08.2024 – 30.09.2025
  Q1 2025: Publication
  Q3 2025: Addendum with **reactions from industry and academia**

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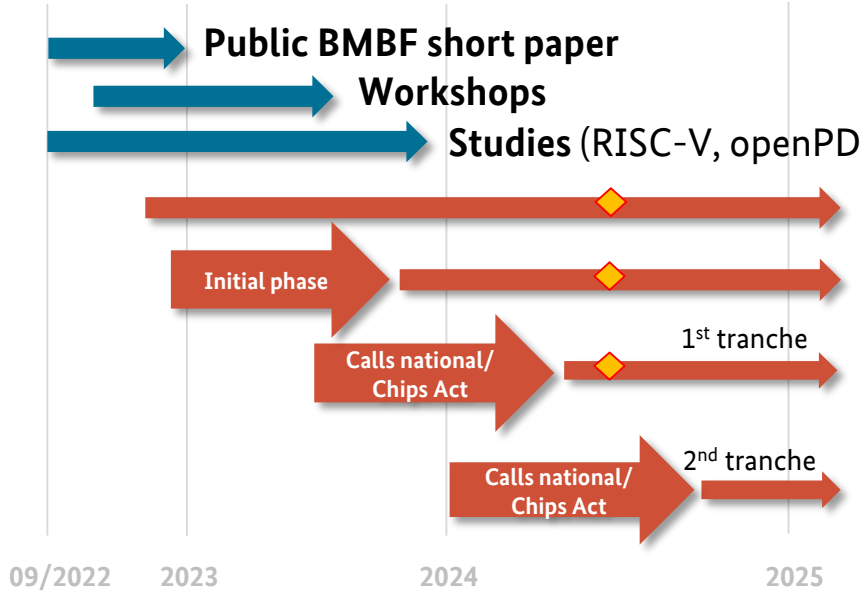
Outlook



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