



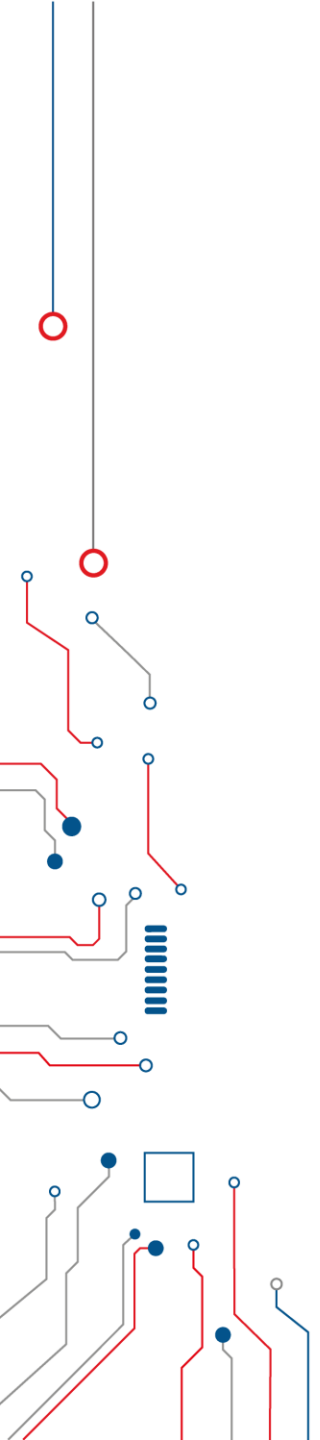
Leibniz Institute
for high
performance
microelectronics

Open source Design Flow status and roadmap for IHP BiCMOS technology

Sergei Andreev – Scientist / Research & Prototyping Service

FSiC2023

July 10 2023



IHP – Institute for High Performance Microelectronics



Main Activities

- μ & nano - Technologies for wireless and broadband communication, health, security, space and industrial automation

Infrastructure

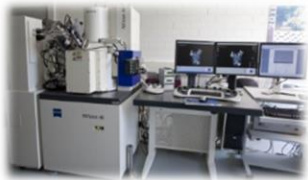
Technology platforms

Service

24/7 operation of 8" Pilot Lines for 130nm SiGe-BiCMOS / EPIC



8" wafer bonding (temporary, permanent, μ TP,..)



Metrology & mmW, THz e/o char.

Qualified

Early Access

Development

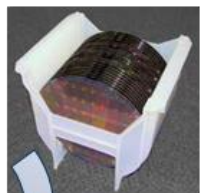
MPW prototyping & LVP



System



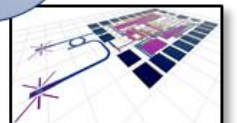
Technology



Circuit



Design

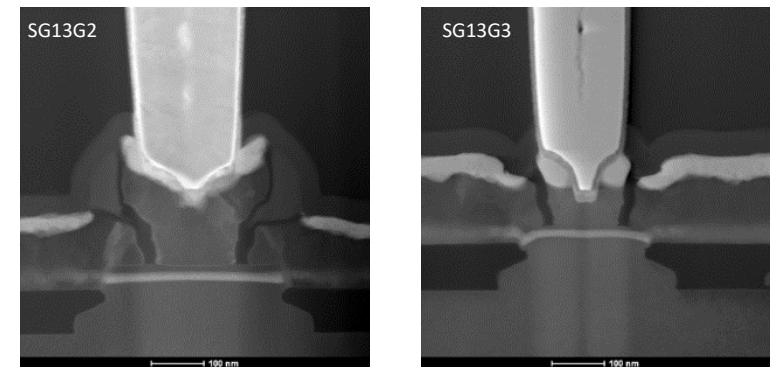
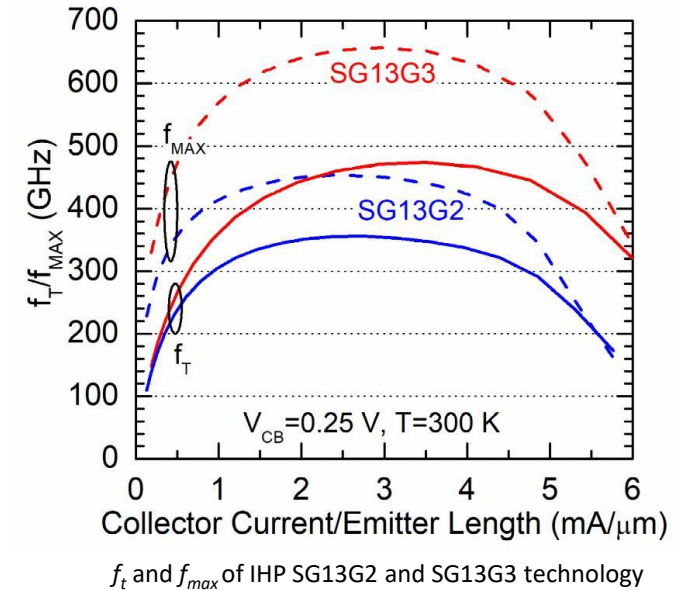


130nm SiGe BiCMOS Technologies for RF Applications



	SG13S	SG13G2	SG13G3
HBT f_t/f_{max}	250 / 340 GHz	350 / 500 GHz	470 / 650 GHz
$W_{Emitter}$	170 nm	130 nm	110 nm
HBT BV_{CEO}	1.7 V	1.6 V	1.5 V
CMOS node	130 nm		
Active devices	Schottky diodes, Antenna diodes, PN diodes, ESD		
Varactors	NMOS Varactor		
Resistors	Poly-Si, Thin Film		Poly-Si
MIM Caps	1.5 fF / μm^2 (Al) 2.1 fF / μm^2 (Cu)	1.5 fF / μm^2 (Al) 2.1 fF / μm^2 (Cu)	2.1 fF / μm^2
Metallization	7 Layers AL incl. 2 & 3 μm layers or *Cu: 4 + 2 (3 μm) Al: 2 (3 μm)	7 Layers AL incl. 2 & 3 μm layers or *Cu: 4 + 2 (3 μm) Al: 2 (3 μm)	*Cu: 4 + 2 (3 μm) Al: 2 (3 μm)

*Cu BEOL from X FAB



TEM cross section of an HBT with elevated extrinsic base regions from (a) the SG13G2 process and (b) a t SG13G3 HBT

- SG13G2 technology was selected for the development of an open source PDK

OpenPDK and OpenTooling – Status



1. Motivation/Goals
2. Planned Open Source EDA Flows
3. Available OpenPDK Data
4. Next Steps / Planned Updates
5. IHP Workshop & Open Questions
6. Outlook



Motivation for IHP's open source PDK initiative



- Provide low threshold access to technology & design data, PDK and design tools for chip designer, technology developer & academic projects
- Pipe cleaning to demonstrate possibilities and convince commercial fabs to support open source approach
- Simplify access to education material for chip designer

- Initiate cooperation's and joint projects with open source community
- Support chip design possibilities for small design projects/companies

German funding from FMD-QNC project



3 Main Tasks:

- Push German Microelectronic Academy – Certified Design Courses & Design Infrastructure using open source
- **Develop Open-Design-Platform / Tooling & PDK**
- Support with Free Area in MPW Runs (chip designs for non-economic activities, such as university education, research projects)

Open PDK & Open Tool Development



- This provides bases for education of designer and design projects
- IHP started on existing experiences of “SkyWater project”
- IHP will dig more in analog design flow, later RF design
- Quality should fulfill requirements for academic education
- Tools must be improved, interface development is crucial

- For a sustainable approach we have to improve capabilities to a level to support productive projects
 - Secure long term funding by MPW & Foundry Service
 - Achieve industrial/non-public funding

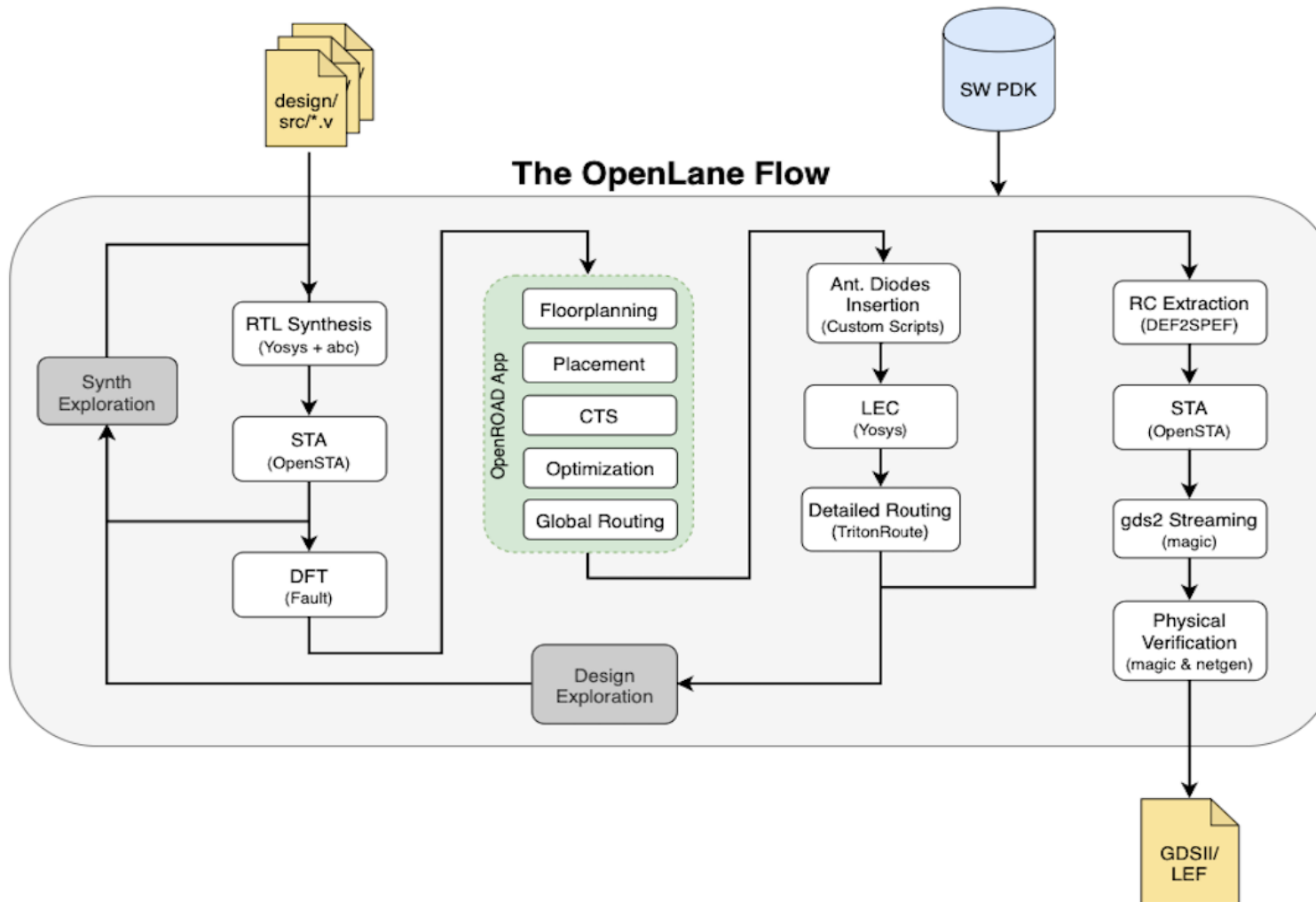
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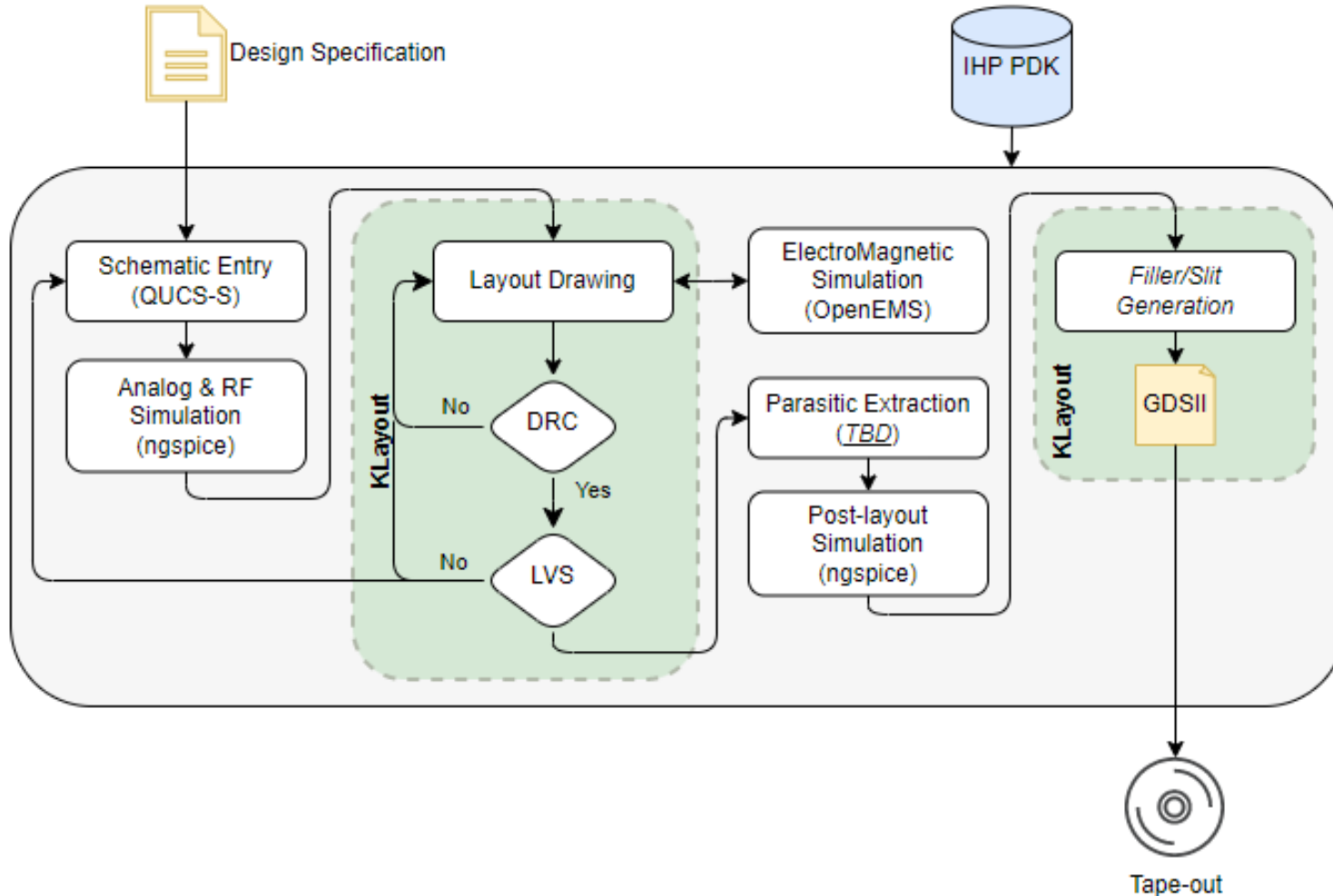


Digital Open Source Development Flow



- Yosys + ABC
- Magic
- Netgen
- CVC
- SPEF-Extractor
- OpenSTA
- KLayout
- Fast/TritonRoute
- TritonCTS
- ...

Analog/RF OpenPDK/EDA Flow



- KLayout-oriented flow
- Layout design
- Parameterizable cells
- Physical Verification
- QUCS-S
- ngspice
- OpenEMS
- ... ?

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Dedicated OpenPDK Virtual Linux Host Machine



- Virtual Machine (VMWare VSphere) with Linux OS
 - 4 CPU
 - Memory 16GB
 - HD 1TB
 - OS Ubuntu 22.04.2 LTS
 - SSH, FTP, ThinLinc servers
 - Only internal users by request
 - Automatic backup every 24h at night
- Base for a small open cloud server scheduled 2024

PDK	sky130 [GitHub, open_pdks]
Layout	KLayout [Deb package, v0.28] Magic [GitHub] KiCAD [6.0.2] gdspy [1.6.12] netgen [GitHub]
Schematic	Xschem [GitHub] QUCS-S [GitHub] Revolution EDA [GitHub]
Simulation	Ngspice [GitHub] Xyce [GitHub] spectre2spice [GitHub]
Modeling	DMT [GitHub, user-level] OpenVAF [23.2.0]
EM	OpenEMS [GitHub] Octave [6.4.0]
Flows	Open_pdks [GitHub, user-level] OpenLane [GitHub, user-level]
PCells	OpenPCells [GitHub, user-level] Magic TCL & KLayout Python Pcells [GitHub, sky130]
Gen	PDKMaster [0.9.0, PyPi]
Documentation	doxygen [1.9.1] graphviz [2.43.0]

OpenPDK Project on GitHub



A screenshot of the GitHub repository page for 'IHP-GmbH / IHP-Open-PDK'. The page shows the repository name, public status, and navigation tabs for Code, Issues, Pull requests, Discussions, Actions, Projects, Wiki, Security, Insights, and Settings. The main content area displays a commit history table with columns for author, message, commit hash, and time. Below the table is the README.md file content, which includes the project title 'IHP Open Source PDK', a description of the 130nm BiCMOS Open Source PDK, the project goal, current status, and a warning about the preview nature of the content. The right sidebar contains repository statistics such as 'About', 'Readme', 'Apache-2.0 license', '149 stars', '22 watching', '10 forks', and 'Releases'.

PDK Contents:

- Project Roadmap Gantt chart
- Base cell set with limited set of standard logic cells (Open130-G2)
- SRAM cells (GDS)
- Primitive devices (GDS)
- KLayout layer property and tech files
- SPICE Models of HBT devices
- OpenEMS: tutorials, scripts, documentation
- SG13G2 Process specification
- SG13G2 Layout Rules
- MOS/HBT Measurements in MDM format

<https://github.com/IHP-GmbH/IHP-Open-PDK>

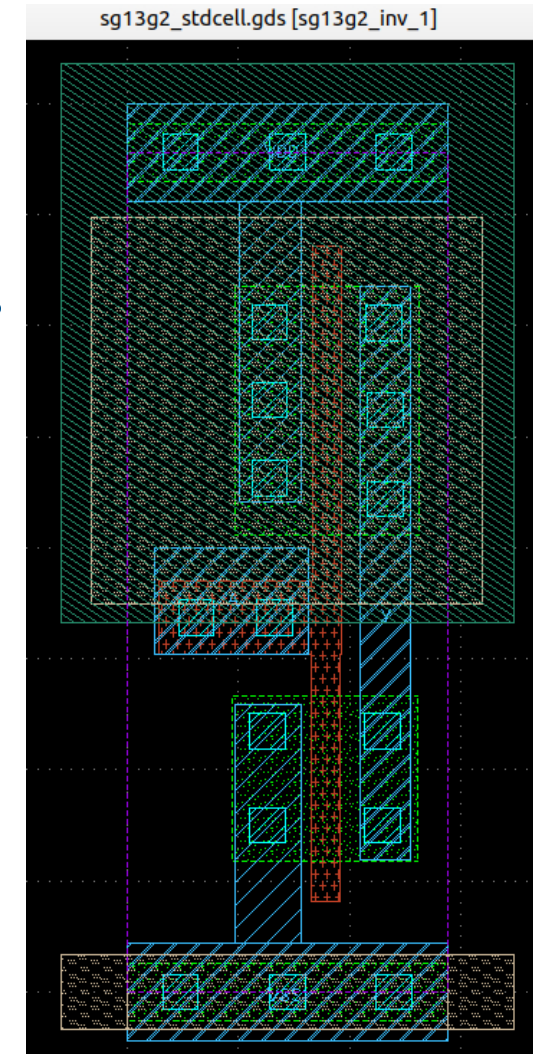
Base Cell Set with Digital Standard Cells



- 78 cells
- Views
 - CDL Netlist
 - GDSII
 - LEF, Tech LEF
 - SPICE Netlist
 - Liberty
 - Verilog
 - OA Library *
- Functions
 - ao[i], [n]and, buf, decap, flops, dly, fillers, inv, mux, [n]or, tie, x[n]or, auxiliary

```
*****  
* Library Name: sg13g2_stdcell  
* Cell Name: sg13g2_inv_1  
* View Name: schematic  
*****  
  
.SUBCKT sg13g2_inv_1 A VDD VSS Y  
*.PININFO A:I VDD:B VSS:B Y:O  
MX1 VSS A Y VSS sg13_lv_nmos m=1 w=740,00n l=130,00n ng=1  
MX0 VDD A Y VDD sg13_lv_pmos m=1 w=1,12u l=130,00n ng=1  
.ENDS
```

```
// type: IN  
'timescale 1ns/10ps  
'celldefine  
module sg13g2_inv_1 (Y, A);  
  output Y;  
  input A;  
  
  // Function  
  not (Y, A);  
  
  // Timing  
  specify  
    (A => Y) = 0;  
  endspecify  
endmodule  
'endcelldefine
```

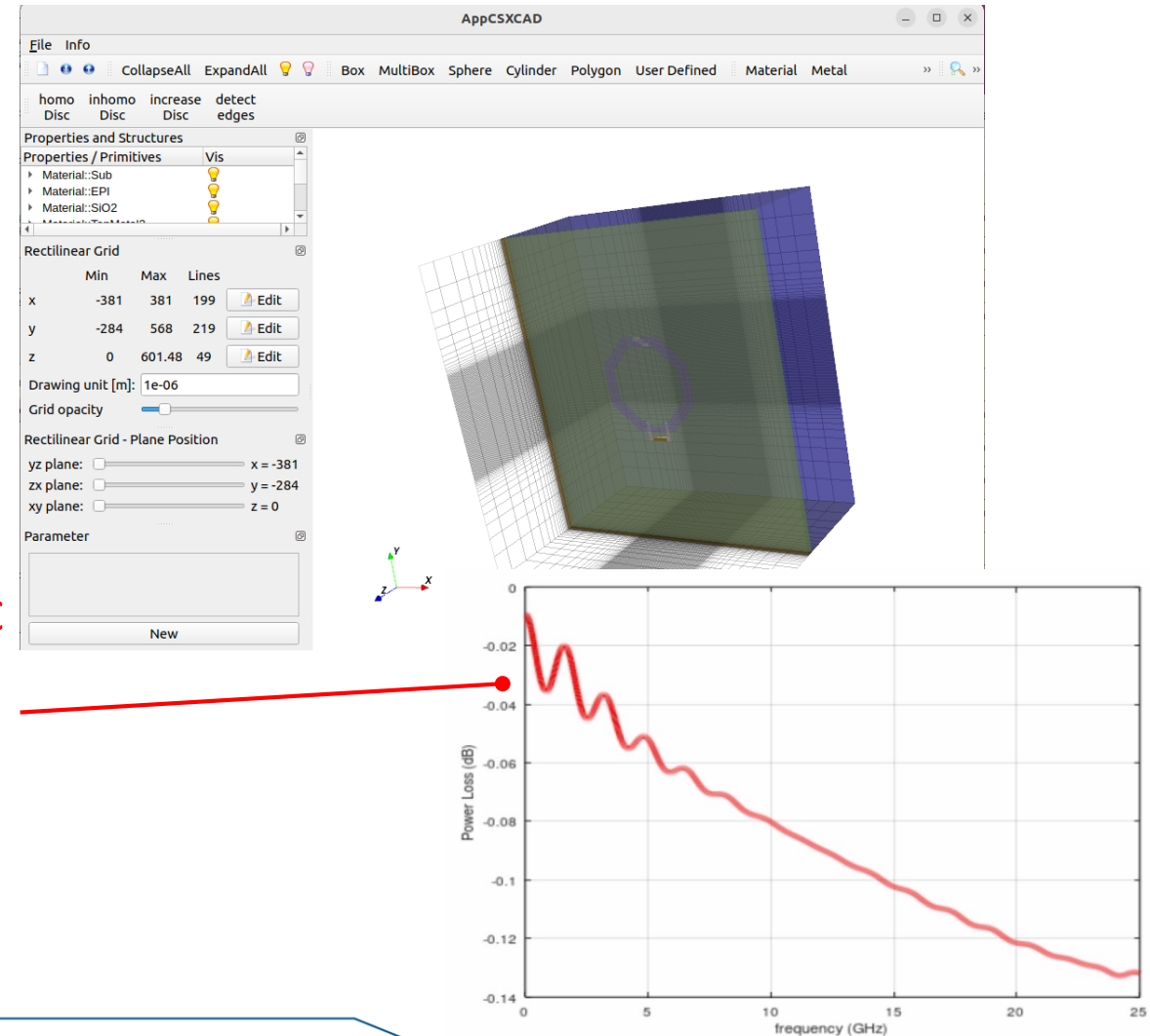


* not part of the OpenPDK delivery

OpenEMS ElectroMagnetic Solver Review



- 3D FDTD solution targeting RF EM simulations
- Model built by Python or Octave/Matlab scripting
- Graphical viewer for model + mesh (CSXCAD)
- Some interfaces to EDA packages, but **no KLayout** support yet
- No internal support for GDSII import, interface was created using Python library gdspsy
- S-Parameter output
- Useful tutorials for RF examples
- Possible issue: small residual energy at low frequency or DC might create DC leakage in simulation results**
- Mostly manual mesh definition**
- No user friendly GUI for IC designer



QUCS-S Custom Library with IHP OpenPDK Devices



The screenshot shows the QUCS-S 1.0.0 software interface. The main window displays a circuit diagram with an input port 'in', a capacitor C1 (0.1 uF), a resistor R3 (24 kOhm), a resistor R1 (2 kOhm), a transistor X1 (npn13G2), a resistor R2 (470 Ohm), a resistor R5 (4.7k), and a capacitor C2 (0.1 uF) connected to an output port 'out'. The transistor X1 is highlighted with a red box. The component libraries on the left are also shown, with 'npn13G2' selected in the 'User Libraries' section. The 'Symbol' section at the bottom left shows the transistor symbol. The bottom of the window contains simulation controls for 'transient simulation' and 'ac simulation'.

```
<Symbol>
<Line -30 0 10 0 #000080 2 1>
<Line -20 0 10 0 #800000 2 1>
<Line 0 -15 0 -5 #800000 2 1>
<Line -10 -5 10 -10 #800000 2 1>
<Line 0 -20 0 -10 #000080 2 1>
<Line -10 5 10 10 #800000 2 1>
<Line -6 15 6 0 #800000 2 1>
<Line 0 9 0 11 #800000 2 1>
<Line 0 20 0 10 #000080 2 1>
<Line -10 0 20 0 #800000 2 1>
<Line 10 0 10 0 #000080 2 1>
<Line -10 -15 0 30 #800000 3 1>
<Text 5 -10 5 #005500 0 "bn">
<.PortSym 0 -30 1 90>
<.PortSym -30 0 2 0>
<.PortSym 0 30 3 270>
<.PortSym 20 0 4 180>
<.ID 10 10 X>
</Symbol>
```

— Directory structure of user lib:

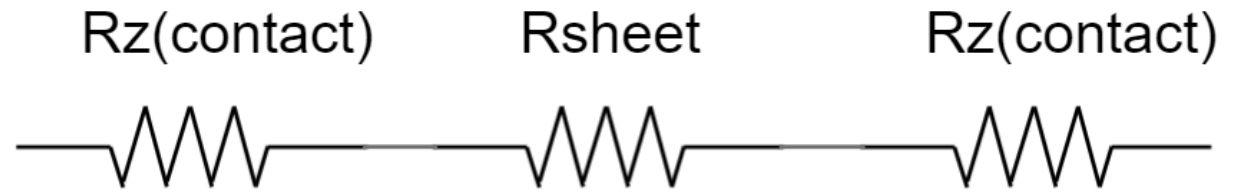
```
~/qucs/
├── user_lib
│   ├── SG13G2_HBT
│   └── SG13G2_HBT.sym
└── SG13G2_HBT.lib*
```

* HSPICE models file from OpenPDK without any modifications

Resistor Models



- Spice Models **Ready** for
 - R_{sil} ($R_s = 7 \Omega/\square$)
 - R_{high} ($R_s = 1360 \Omega/\square$)
 - R_{ppd} ($R_s = 260 \Omega/\square$)
- Temperature Modeling ✓
- Noise Modeling ✓
- Ngspice, Xyce compatible ✓
- Non-linear effects not included: ✗
 - Self heating
 - Velocity saturation
 - ...
- Working on adapting **R3 CMC** resistor model.



Simple linear spice semiconductor resistor model

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Next Steps / Planned Updates



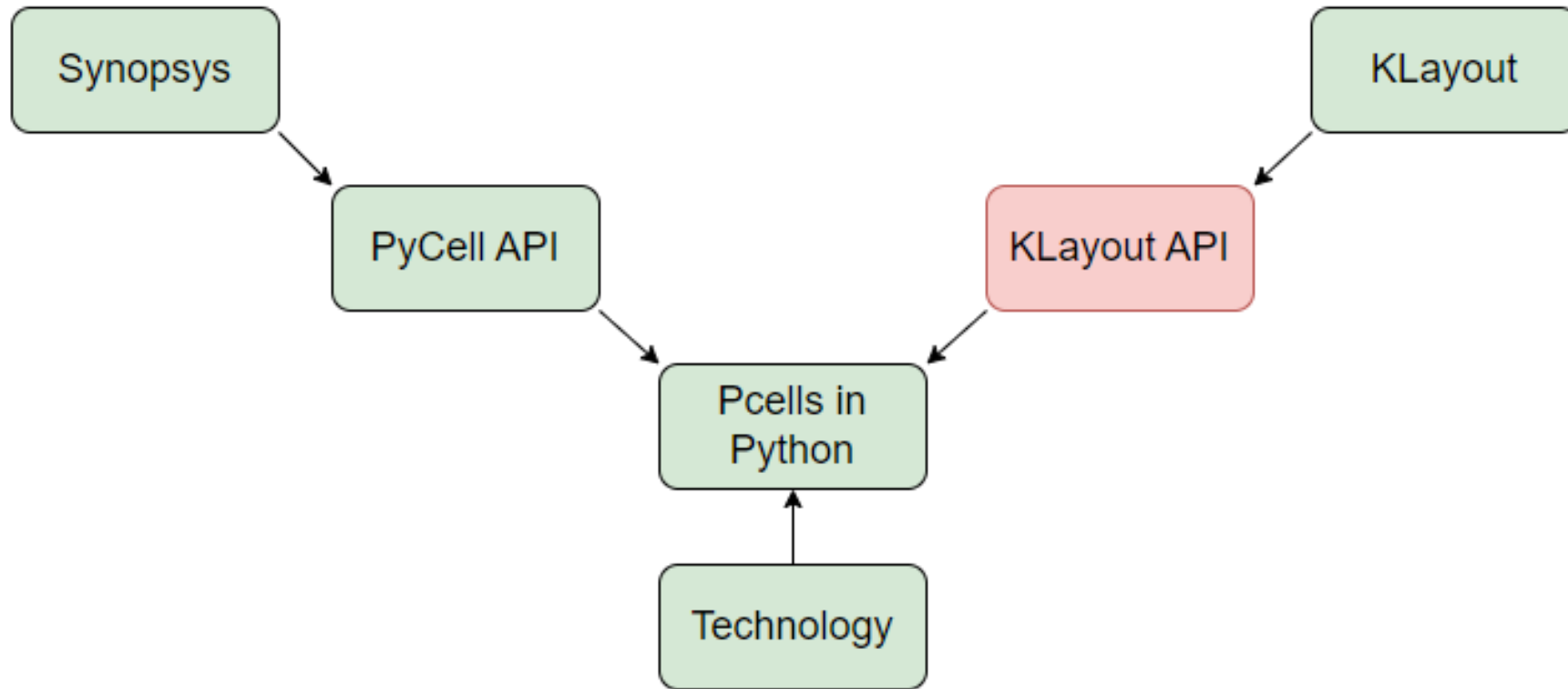
- Start set of Digital cells
 - Additional cells in development by ETH Zurich + community
- IO cells
- LEF view for primitive devices
- KLayout Technology file
 - Add connectivity section
- **Need help on:**
 - **MOS SPICE models**
 - **PCells**

–○ Tasks on GitHub:

	Title	...	Status
1	Ngspice: 'ignored parameter' messages for HBT models		Done
2	Start set of Digital cells		Done
3	Digital standard cells enhancements (increased set)		In Progress
4	IO cells		Todo
5	SRAM cells		Done
6	LEF view for primitive devices		Todo
7	MOS HSPICE models		Todo
8	KLayout Tech file		Done
9	DRM for Opensource PDK		Done
10	QUCS-S Library w/ IHP OpenPDK devices		In Progress
11	Move documentation to ReadTheDocs framework		Todo
12	PyCells		Todo

- SG13G2 MOS Spectre models to SPICE format conversion to use with ngspice/Xyce simulators
 - supported:
 - extreme value behavior, corner cases
 - transistor layout data transfer
 - drain/source area calculations using the fingers number
 - some Spectre commands/instructions/statements not supported:
 - geometry checks
 - static and dynamic states checks
 - statistical variations

—○ SG13G2 Synopsys PyCells to KLayout Python Pcells conversion



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OpenPDK Workshop at IHP

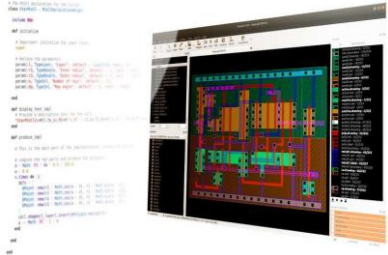


- **OpenPDK, OpenTooling and Open Source Design – An Initiative to Push Development**
 - 2-day workshop on 27/28 June @Frankfurt (Oder)
 - Promote exchange and networking
 - Designers present ideas to educate chip designers
 - Tool developers present tool features / planned enhancements
 - Agenda with uploaded slides on GitHub Wiki:
<https://github.com/IHP-GmbH/IHP-Open-PDK/wiki/Networking-Workshop-FMD-QNC>
 - **Goals:**
 - Identify / prioritize gaps in design flow
 - Help plan the OpenPDK project roadmap

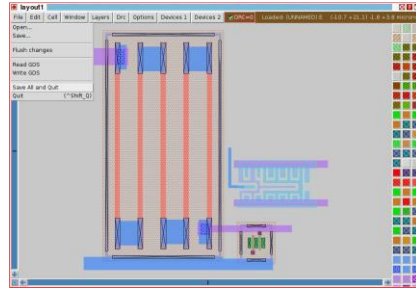
Tool support questions



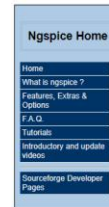
○ KLayout



○ Magic



○ ngspice



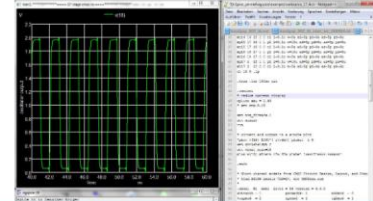
ngspice - open source spice simulator

ngspice is the open source spice simulator for electric and electronic circuits.

Such a circuit may comprise of JFETs, bipolar and MOS transistors, passive elements like R, L, or C, diodes, transmission lines and other devices, all interconnected in a netlist. Digital circuits are simulated as well, event driven and fast, from single gates to complex circuits. And you may enter the combination of both analog and digital as a mixed-signal circuit.

ngspice offers a wealth of device models for active, passive, analog, and digital elements. Model parameters are provided by our [collections](#), by the [semiconductor device manufacturers](#), or from [semiconductor foundries](#). The user adds her circuits as a netlist, and the output is one or more graphs of currents, voltages and other electrical quantities or is saved in a data file.

ngspice does not provide schematic entry. Its input is command line or file based. There are however [third party](#) interfaces available.



○ Xyce

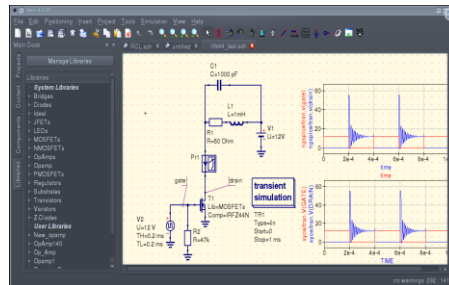


About Xyce

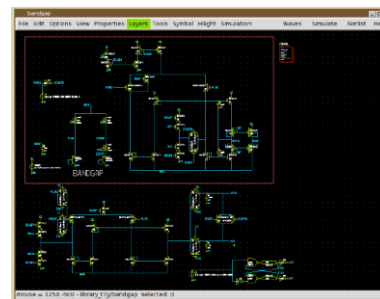
Xyce is an open source, SPICE-compatible, high-performance analog circuit simulator, capable of solving extremely large circuit problems by supporting large-scale parallel computing platforms. It also supports serial execution on all common desktop platform small-scale parallel runs on Unix-like systems. In addition to analog electronic simulation Xyce has also been used to investigate more general network systems, such as neural networks and power grids. [Read more about Xyce.](#)



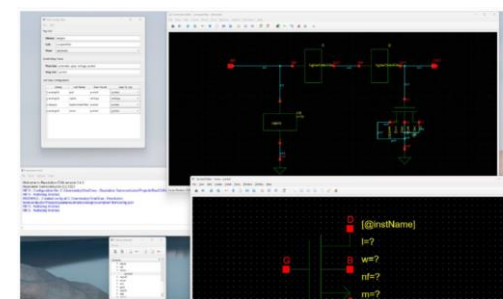
○ QUCS-S

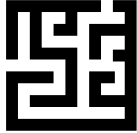
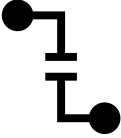
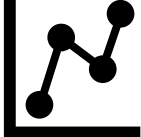


○ Xschem



○ RevolutionEDA



- Questions about tool support answered:
 - Layout Design: KLayout **and** Magic 
 - Circuit Design: QUCS-S **and** Xschem 
 - Simulation: ngspice **and** Xyce 

Workshop Results (continued)



- Open discussion/issues:
 - Documentation of tools must be improved!
 - Lacking functionality here and there, interface missing between some tools
 - Simple GUI for attracting a broader community, BUT cmd line more important → functionality and productivity
 - More focus on standard files exchange format instead of common DB
 - Test cases!! → Open Source PDK → Start improvement cycle
 - Resources and planning for open source tools is a **problem**, joint strategy?
 - Foundation (European?) for open EDA tools

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Open Source Roadmap



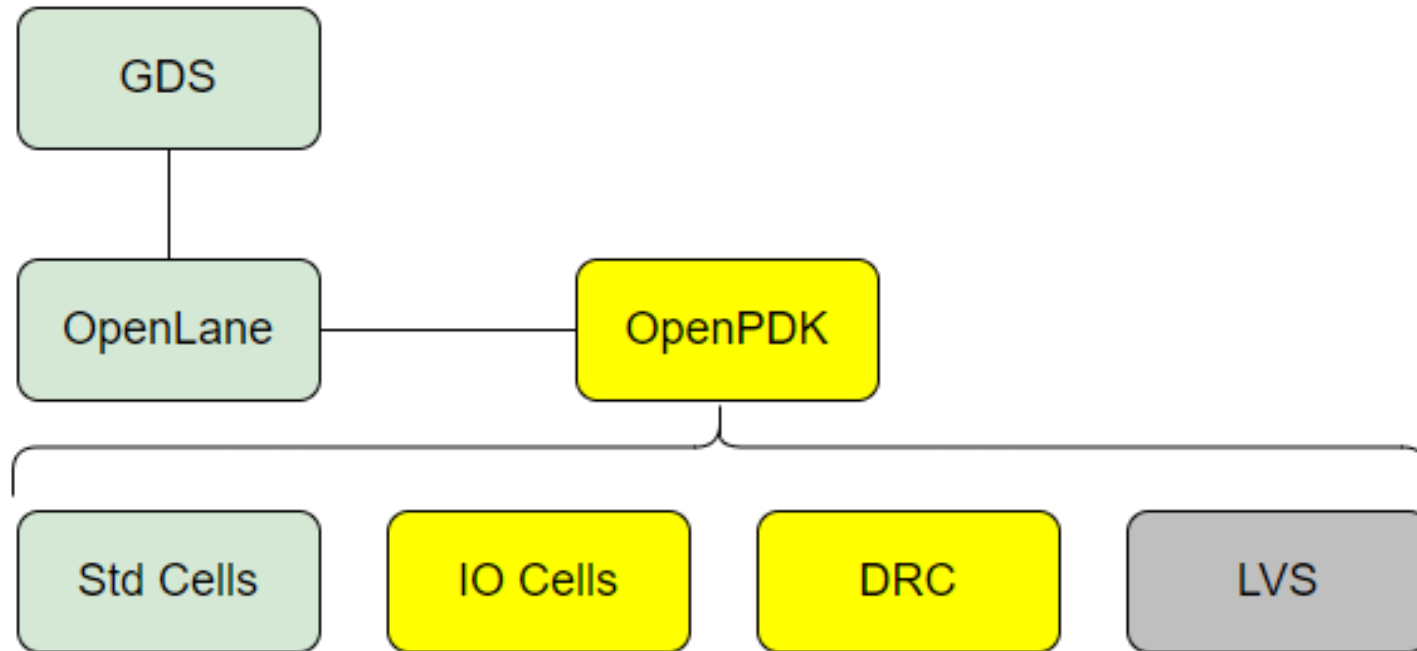
- Agree on common goals for a design flow – to channel effort
- Synchronize efforts and tasks, review/update project schedule
- Leveraging community efforts, public funding and corporate contributions

- Demonstration of successful open source designs
- Demonstration of design training courses in academic institutions
- Example for a commercial successful project

First phase target



➔ Submit digital design based on open PDK in Dec Y23



- Legend:
- available
 - in progress
 - tbd

Acknowledgment



- Thanks to my colleagues at IHP
- Thanks to ETH Zurich + open source community
- Separate thanks to Volker Mühlhaus for work on the EM solvers
- And final thanks to different public founded German projects:
 - VE-HEP (16KIS1339K) <https://elektronikforschung.de/projekte/ve-hep-1>
 - IHP Open130-G2 (16ME0852) <https://www.elektronikforschung.de/projekte/ihp-open130-g2>
 - FMD-QNC (16ME0831) <https://www.elektronikforschung.de/projekte/fmd-qnc>
 - Workshop funding - FMD-QNC with VDI/VDE (project management agency) approval

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Thank you for your attention!

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