A Yosys plugin for logic locking

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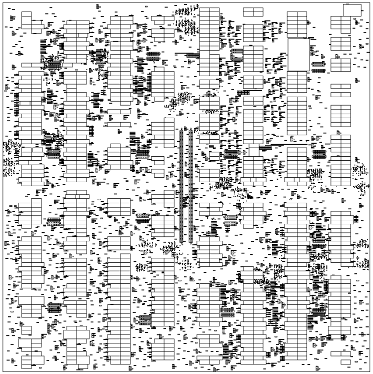
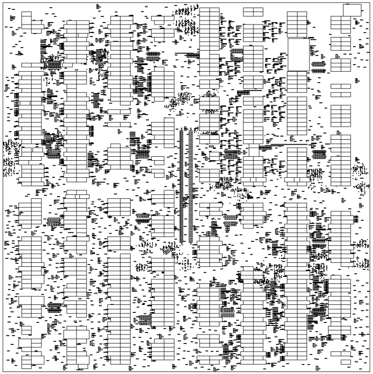
EDA Projects



Coloquinte: Coriolis placement tool

EDA Projects



Coloquinte: Coriolis placement tool

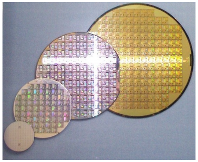
Moosic: This presentation

- Presented last year by Roselyne Chotin and Lilia Zaourar
- This year: integration in Yosys

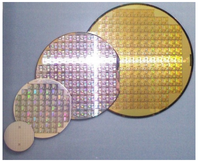
FSiC2022
Free Silicon Conference

Supply-chain security for integrated circuits

Most circuit conception is fabless



Supply-chain security for integrated circuits



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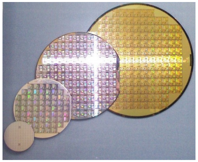
You trust the fab and tools not to:

Supply-chain security for integrated circuits



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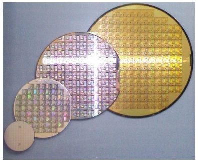

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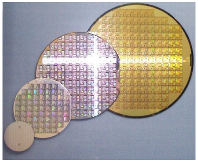

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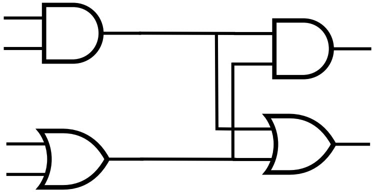
How?

Logic locking example



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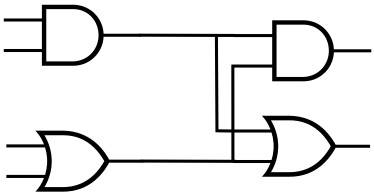

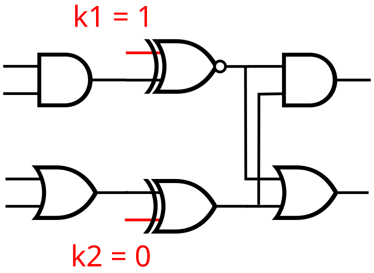

Logic locking

Add logic that doesn't work without the right key

Simple method: Xor/Xnor gate insertion

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- Mangling $\Rightarrow$ mitigates trojans

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Can we attack it?

Guessing the key: structural approaches

By default, keys are easy to find:

- Xor $\rightarrow$ 0 key
- Xnor $\rightarrow$ 1 key

Defense:

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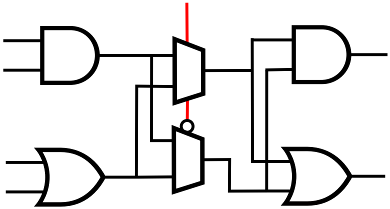

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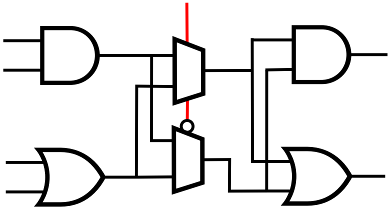
ML attacks may still break those



Finding the key: SAT attack

Expected behaviour + logic circuit

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⇒ SAT problem

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- More complex locking

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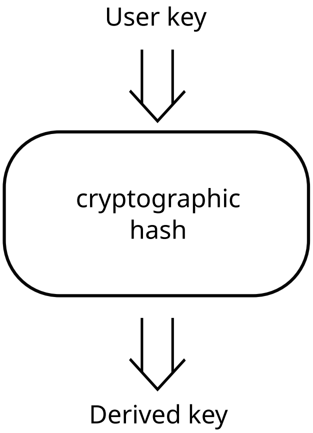
- Better choice of locked signals

Finding the key: SAT attack

Expected behaviour + logic circuit
⇒ SAT problem

Defense:

- More complex locking
- Better choice of locked signals
- Derived keys (crypto...)



What makes a good logic locking?

Hard to guess the key

Disrupts circuit functionality

Mixed with the logic

Metrics

Metrics

Output corruption: the wrong key changes many output values

Metrics

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Pairwise security: key bits cannot be silenced individually

Why a Yosys plugin

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Open-source existing research

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Large ecosystem

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Open-source existing research

Large ecosystem

Easy to install and integrate

Plugin functionalities

Xor- and Mux- based logic locking

Automation of Xor-based logic locking (metrics)

Design space exploration (area vs security)

Not included

Not included

Key handling left to the user

- Too HW-dependent (memory, boot, scan-chain...)
- Linked to crypto primitives

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No attack methods (ML or SAT)

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Only flat modules

In practice

Number of signals to lock

Number of test vectors

Metrics

Design space exploration?

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Number of signals to lock

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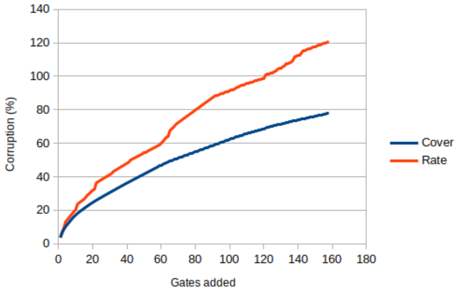
Design space exploration?



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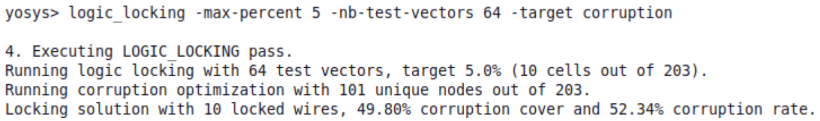

```
yosys> logic_locking -max-percent 5 -nb-test-vectors 64 -target corruption

4. Executing LOGIC_LOCKING pass.
Running logic locking with 64 test vectors, target 5.0% (10 cells out of 203).
Running corruption optimization with 101 unique nodes out of 203.
Locking solution with 10 locked wires, 49.80% corruption cover and 52.34% corruption rate.
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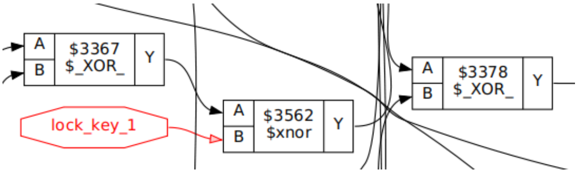

Next steps

Connect with users:

Research: metrics implementation and evaluation

Thank you

https://github.com/Coloquinte/moosic-yosys-plugin