

# From filters to transistors

A library of analog schematic with automated sizing

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CIAN Team: FOSS EDA for analog and mixed circuit design

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# Plan

- 1 Sizing and characterizing a MOS transistor
- 2 Sizing and characterizing a Miller amplifier
- 3 Sizing and characterizing an elliptic Filter
- 4 Conclusion

1 Sizing and characterizing a MOS transistor

2 Sizing and characterizing a Miller amplifier

3 Sizing and characterizing an elliptic Filter

4 Conclusion

# Analog Design : biasing, sizing and characterizing the MOS transistor

- MOS calculator

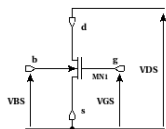
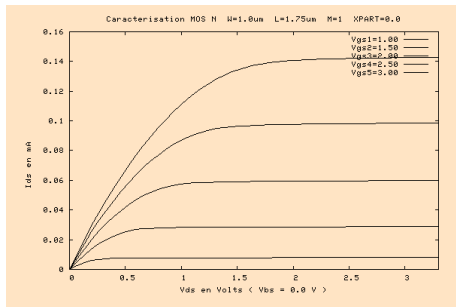


FIGURE: MOS transistor with its 4 terminals : gate, drain, source, bulk.

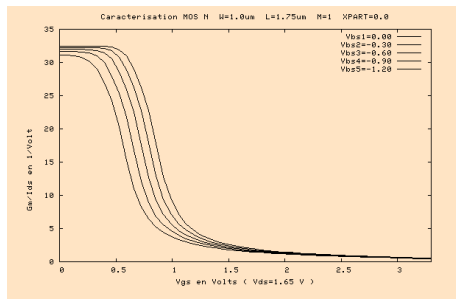
- ▶ MOS **models** (equations) : BSIM, ...
- ▶ + **process** parameters (foundry, technology nodes)
- ▶ **analysis** :  $I_{DS}$  is computed
$$I_{DS} = f_{(model,process)}(W, L, V_{GS}, V_{DS}, V_{BS}, temp)$$
- ▶ MOS **regime** :
  - $V_{OV} = V_{GS} - V_{TH}$ , overdrive voltage, inversion mode
  - $V_{Dsat} = V_{GS} - V_{TH}$ , saturation/linear
- ▶ **sizing** :  $W$ ,  $L$  or  $V_{GS}$  are **computed**
  - set  $V_{OV}, W, L \Rightarrow I_{DS}, V_{GS}$
  - set  $V_{OV}, I_{DS}, L \Rightarrow W, V_{GS}$
  - set  $V_{OV}, I_{DS}, W \Rightarrow L, V_{GS}$

# MOS transistor calculator

Analyzing the MOS transistor :  $I_{DS}(V_{DS})$  and  $\frac{G_m}{I_{DS}}(V_{GS})$



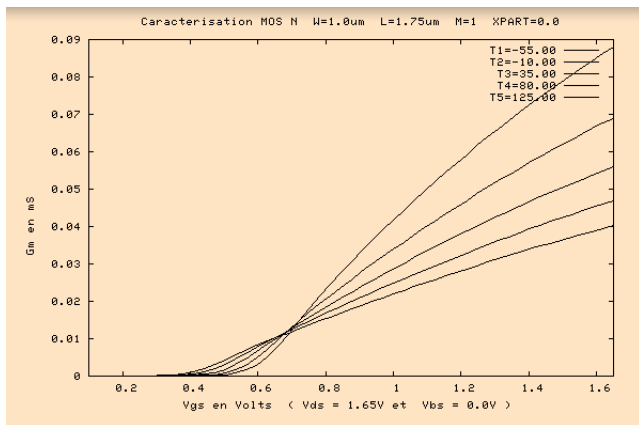
**FIGURE:** MOS transistor. Drain current  $I_{DS}$  versus drain source voltage  $V_{DS}$ .  
 $I_{DS} = f(W, L, V_{GS}, V_{DS}, V_{BS}, temp)$



**FIGURE:**  $G_m$  over  $I_{DS}$  versus  $V_{GS}$ , for various  $V_{BS}$ . Image of the overdrive voltage ( $2/V_{OV}$ ).

# MOS transistor calculator

Sizing the transistor for the optimal overdrive voltage  $V_{OV}$  :



**FIGURE:** Transconductance  $G_m$  versus  $V_{GS}$ , for different temperatures in the range  $[-55^\circ\text{C}, 125^\circ\text{C}]$ . Selection of the optimal point :  $V_{OV} \sim 0.2$  V, according to temperature variation.

# MOS transistor calculator within Oceane

**Parametrage de la netlist**

nom du dispositif: MN1  S  T  F

label D: d label G: g label S: s label B: b

WF	1.05	WF	1.05
L	1.75	L	1.75
M	1	M	1
ID	1.90793e-06	ID	1.90792e-06
VGS	7.28904e-01	VGS	7.28904e-01
VDS	1.65000e+00	VDS	1.65000e+00
VBS	0.00000e+00	VBS	0.00000e+00
VTH	5.08831e-01	VTH	5.08904e-01
VON	5.08831e-01		

**Selection du parametre a calculer**

- calcul du courant drain-source
- calcul de la largeur WF
- calcul de la longueur L
- calcul de la tension grille-source avec  $v_{gs} = v_{ds}$
- calcul de la tension grille-source avec  $v_{gs} \ll v_{ds}$

**Entree des parametres de calcul**

longueur du transistor (L en um) : 1.75

largeur d'un doigt (WF en um) : 1.05

nombre de doigt par engilage (NF=M) : 1

tension grille-source (VGS en V) : 7

tension effective de grille (VEG en V) : 0.22

tension drain-source (VDS en V) : 1.65

tension substrat-source (VBS en V) : 0.0

courant drain-source (IDS en uA) : 1.9

temperature de calcul : 27

centrage technologique (nb sigma) : 0.0

XPART :  0  0.5  1

selection des parametres technologiques: VTH: 1

**Entree des parametres de layout & de style**

SET  GEOMOD: 0  RGEOMOD: 0  NGCON: 1

Calcul par COMDIAC      Calcul par SIMULATEUR

FIGURE: Oceane MOS transistor sizing (i.e. set  $V_{OV}$ ,  $I_{DS}$ ,  $L \Rightarrow W$ ,  $V_{GS}$ ) and characterizing cockpit. Oceane and ns spice results are equal.

# Behind the MOS transistor cockpit

- **Oceane/COMDIAC** built-in MOS transistor models

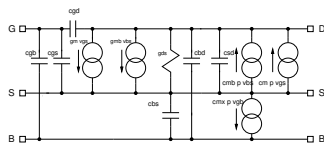


FIGURE: Small signal equivalent schematics.

- **Complete** MOS transistor model (as in simulator)
- Official parameters of the **BSIM3/4** models (NDA)

- **all parameters** are taken into account :
  - ▶ layout dependent parameters
  - ▶ Stress effect
  - ▶ multi  $V_{TH}$
- **ngspice** simulator is called to validate each design
- a library of configurable **test benches** is available
- DC operating point, transient analysis, and AC analysis can be performed.



- 1 Sizing and characterizing a MOS transistor
- 2 Sizing and characterizing a Miller amplifier**
- 3 Sizing and characterizing an elliptic Filter
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# Analog Design : biasing, sizing and characterizing the Miller amplifier

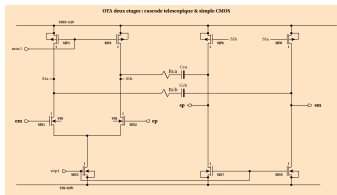


FIGURE: 2 stage Miller amplifier. Several topological alternatives are provided.

- Selection of **topology**, with **several alternatives**
  - ▶ Differential pair : NMOS/PMOS
  - ▶ Cascode
  - ▶ Compensation : C alone, R and C
  - ▶ Common mode rejection circuit for differential structures
  - ▶ ...
- **Specifications** (a small set)
- **Computation** (fast to be iterated)
  - ▶ Launched from GUI
  - ▶ or C file
  - ▶  $\Rightarrow$  W,L, R and C
- **Computed performances** (**Maxima**, building symbolic transfer functions)
- **Simulated performances** (validation)

## Sizing Principle : Amplifier case study.

- 1 level 1 MOS transistor **model**, used to illustrate the main steps :  
 $I_{DS} = \frac{\mu}{2} C_{ox} \frac{W}{L} (V_{OV})^2 (1 + \lambda \cdot V_{DS})$ , with  $V_{OV} = (V_{GS} - V_{TH})$  (1)
- 2 **Specification** of the power  $\Rightarrow I_{DS}$ , the biasing **current**  
or Unity Gain Frequency :  $F_U \sim \frac{g_m}{2\pi C_L}$
- 3 The **inversion** level :  $V_{OV} \Rightarrow g_m = \frac{2I_{DS}}{V_{OV}}$ , the transconductance
- 4 **Gain** specification :  $A_{d0} \sim \frac{g_m}{g_{ds}} \sim \frac{L \cdot V_E}{V_{OV}} \Rightarrow L$  since  $\lambda = \frac{1}{L \cdot V_E}$
- 5 Transistor **sizes**, **computed** from Eq. 1 (step 1)
- 6 Secondary performances : input thermal noise  $\sim \frac{K \cdot Temp}{g_m}$ , possible iteration (step 4)
- 7 **Test benches** for performance simulation ( $\sim$  computed ones)

### Oceane

Complete MOS transistor models are used instead of Eq. 1 in Step 1, so that a perfect matching between Oceane and **ngspice** is achieved.

# Analog Design : sizing the Miller amplifier

GUI with input and output files :

tension d'alimentation superieure (VDD en V):   
 tension d'alimentation inferieure (VSS en V):   
 gain statique (A0 en dB):   
 marge de phase (MP en degre):   
 courant de polarisation IP (2.ID\_MN1 en uA):   
 fréquence de transition (FT en MHz):   
 capacité de charge (CL en pF):   
 résistance de charge (RL en KOhm):   
 nombre de dispositifs en parallèle:

tension d'entree de mode commun (VEMC en V) =   
 tension de sortie de mode commun (VSMC en V) =

nom du dispositif: netlist:

label VDD:	<input type="text" value="evdd"/>	label VSS:	<input type="text" value="evss"/>
label IP:	<input type="text" value="ip"/>	label EM:	<input type="text" value="em"/>
label EPD:	<input type="text" value="epd"/>	label EMG:	<input type="text" value="emc"/>
label IP:	<input type="text" value="ip"/>	label SM:	<input type="text" value="sm"/>
label VBN:	<input type="text" value="evbn"/>	label VBP:	<input type="text" value="evbp"/>
label VP1:	<input type="text" value="evp1"/>	label VP3:	<input type="text" value="evp3"/>
label VP5:	<input type="text" value="evp5"/>	label VP6:	<input type="text" value="evp6"/>
label VC1:	<input type="text" value="evc1"/>	label VC3:	<input type="text" value="evc3"/>
label VSMC1:	<input type="text" value="evmc1"/>	label NMC1:	<input type="text" value="emc1"/>
label NMCc:	<input type="text" value="emcc"/>	label NMC3:	<input type="text" value="emc3"/>

FIGURE: Milller amplifier specifications, input file

VP1	0.74765
VP3	2.35770
VSMC1	2.36589
Cc	2.530738e-12
Rc	9.083894e+02

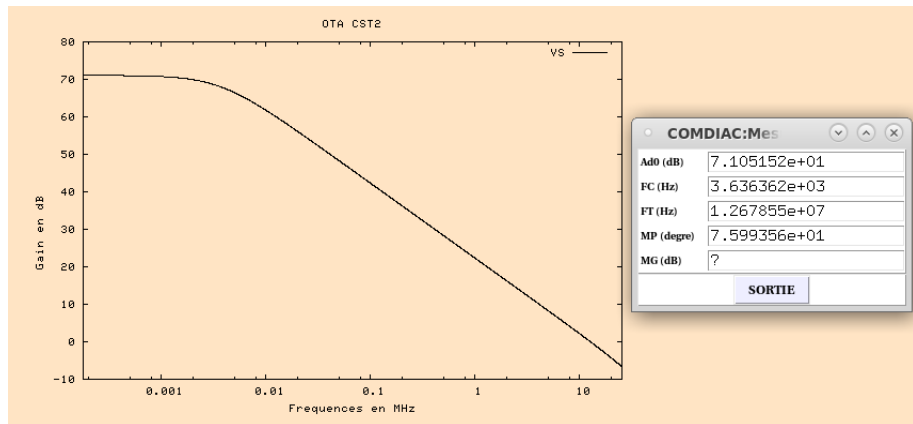
	M	W	/	L
MN1 =	2	2.5750	/	0.6250
MN2 =	2	2.5750	/	0.6250
MP3 =	4	3.7500	/	0.6250
MP4 =	4	3.7500	/	0.6250
MN5 =	4	2.7750	/	0.6250
MP6 =	20	3.7500	/	0.6250
MN7 =	16	1.6000	/	0.6250
MP8 =	20	3.7500	/	0.6250
MN9 =	16	1.6000	/	0.6250

FIGURE: Milller amplifier MOS sizing, output file

A0 (dB) =	71.07
FT (MHz) =	12.71196
MP (degre) =	75.96
SR (V/us) =	8.87e+00
Ac0 (dB) =	-45.06
RRMC (dB) =	116.13
ED0 (fV) =	0.00000
Sigma_ED0 (mV) =	7.80360
VEMCmax =	3.123
VEMCmin =	0.910
VSmax =	3.517
VSmin =	0.895
Rs (KOhm) =	119.53330
Cs (pF) =	2.81979
Ce (fF) =	28.52957
vne(th) (V/Hz) <sup>1/2</sup> =	5.45e-11
vne(1/f) (V/Hz) <sup>1/2</sup> a 1Hz =	3.02e-08
vne(1/f) (V/Hz) <sup>1/2</sup> a FT =	8.48e-12
I0tot (uA) =	299.89130

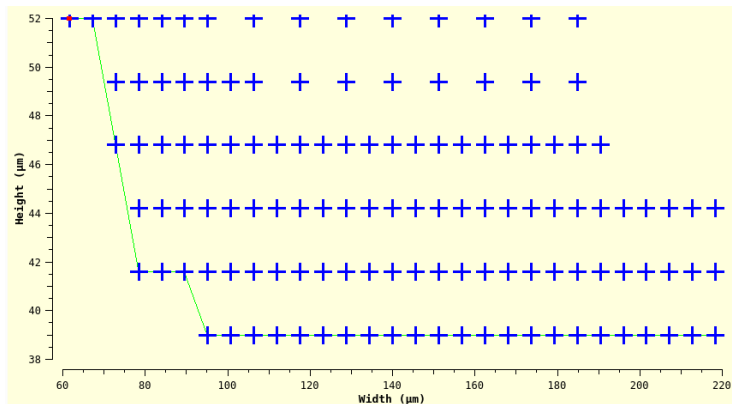
FIGURE: Milller amplifier performances, output file

# Validation of the Miller design with **ngspice** simulation



**FIGURE:** Gain (dB) versus frequency, **ngspice** simulation results, same as computed performances.

# Layout of the Miller design with Coriolis



**FIGURE:** Shape Function, computed by varying the number of transistor folds, for each transistor, of a netlist sized with [Oceane](#).

# Layout of the Miller design with Coriolis

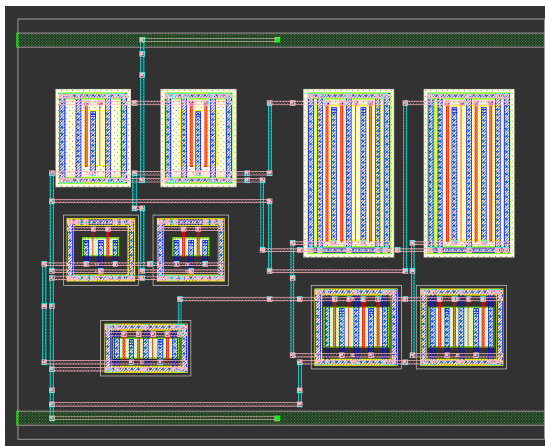


FIGURE: Layout of the square shape, transistor part, sized with **Oceane**.

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# Filter specification

Specifications de gabarit

Type de gabarit

- Passe-bas
- Passe-haut
- Passe-bande
- Coupe-bande

Fonctions modeles

- Bessel
- Butterworth
- Tchebycheff
- Tchebycheff inverse
- Cauer

Gabarit standard passe-bas

Graph showing magnitude response (dB) vs frequency (f). The graph displays a low-pass filter characteristic with a passband gain  $a_{max}$ , a stopband gain  $a_{min}$ , a passband edge frequency  $f_p$ , and a stopband edge frequency  $f_n$ .

ordre = 5

amax en dB = 0.1

amin en dB = -40

fp en Hz = 1e06

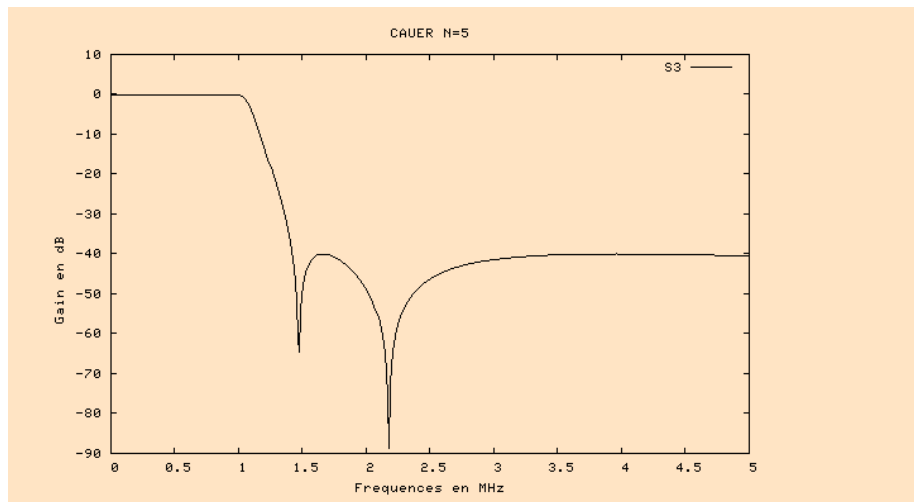
fn en Hz = 1

CALCUL SORTIE

- Type of filtering transfer function :  
Low-pass / band-pass / high-pass
- Specifications (a small set) :
  - ▶ Order of the transfer function (TF)
  - ▶ Frequency boundaries
  - ▶ Gain boundaries
  - ▶ Response shape :
    - ★ Chebyshev
    - ★ Butterworth
    - ★ Bessel
    - ★ Elliptic filter or Cauer filter

FIGURE: Filter specifications

## Transfer function : Cauer, order 5



**FIGURE:** Transfer function of the filter : Gain (dB). Ideal models (OTA, R and C are used)

# Filter design : cascade of 1st order cell and 2 biquad cells

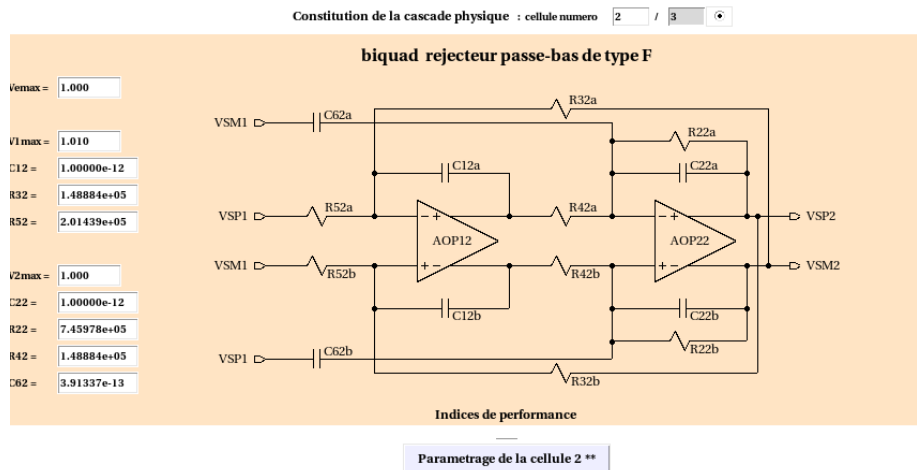
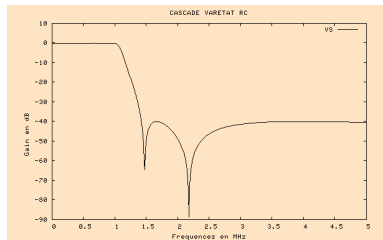
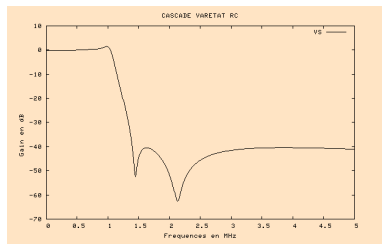


FIGURE: Second cell of the cascade (order 2)

# Filter design with 3 cascaded cells : amplifier specifications



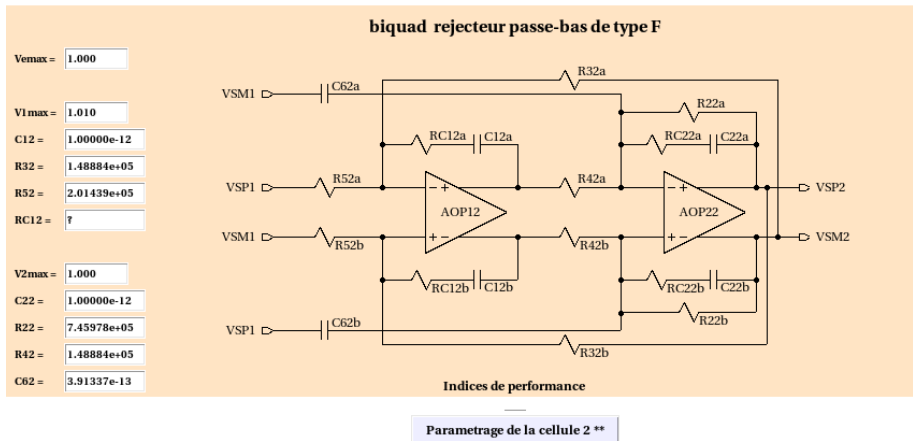
**FIGURE:** Transfer function of the filter : Gain (dB). Macromodels (OTA) are used with **stringent specifications** to fulfill the filter specifications  $\Rightarrow$  **high power consumption**.



**FIGURE:** Transfer function of the filter : Gain (dB). Macromodels (OTA) are used with **relaxed specifications** to decrease the whole power consumption  $\Rightarrow$  **Filter TF error**.

# Filter design : cascade of biquad cells, optimization

Constitution de la cascade physique : cellule numero  /



**FIGURE:** 2<sup>nd</sup> cell of the cascade (order 2) modified to lower the filter power consumption. The low amplifier gain impact is corrected by **resistors in series**, (variant available).

## Transfer function : cascade of biquad cells, validation

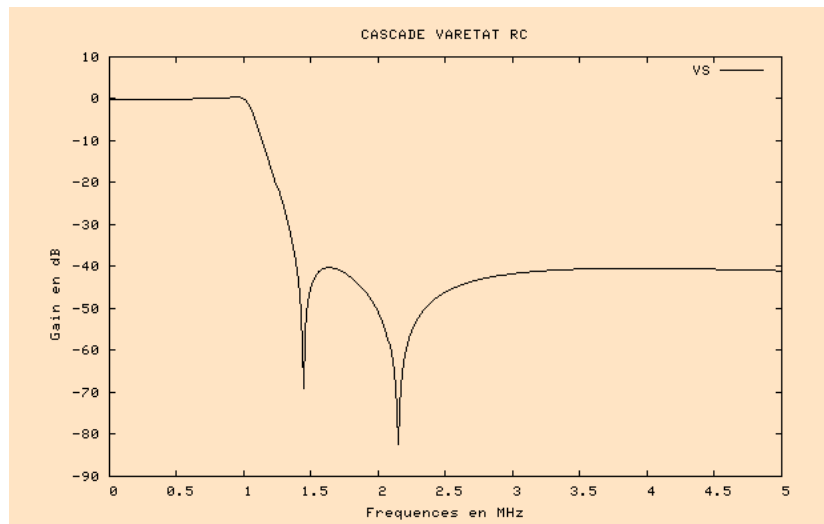
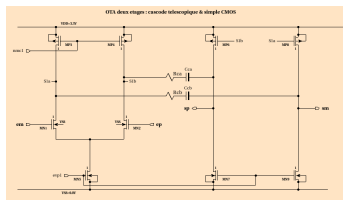


FIGURE: Validation by **ngspice** simulation (macro models of the amplifiers with relaxed specifications and correction)  $\Rightarrow$  correction of the Filter TF.

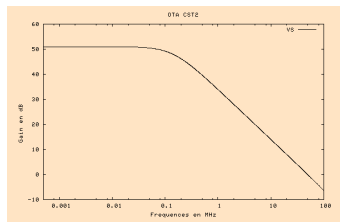
# Filter : cascade of biquad cells, Miller amplifier at transistor level

## Transistor Level and symbolic computation

Complete MOS transistor models are taken into account to compute the symbolic TF of the filter, to achieve a perfect matching between Oceanic computed performances and **ngspice** simulation.



**FIGURE:** Milller amplifier, sized with specifications coming from the macro-model based biquad



**FIGURE:** Milller amplifier gain

# Transfer function : cascade of biquad cells, transistor level

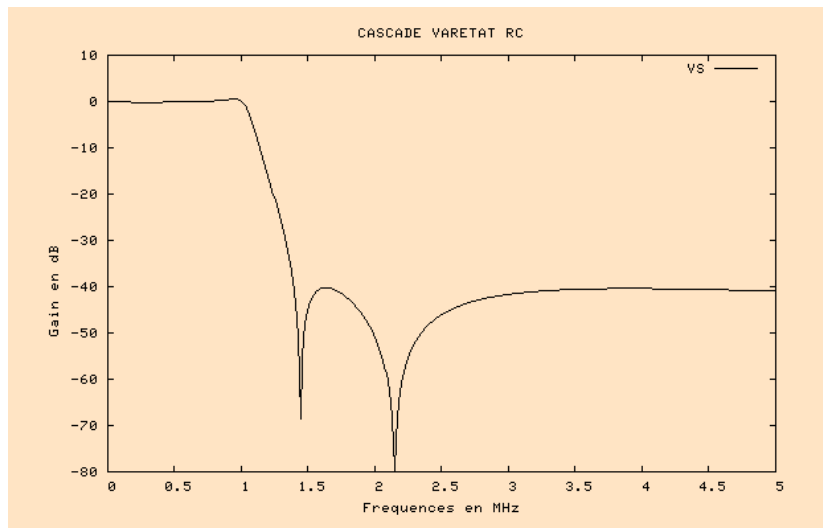


FIGURE: Validation by **ngspice** simulation (full transistor netlist.)



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- **Filter design** : from specifications to transistor netlist.
- **Accurate sizing**, based on the same complete MOS transistor model (BSIM3/4, ...) than the simulator, to ensure accurate sizing.
- Transistor sizing is based on the **overdrive voltage** (independent of the process to ensure technology migration).
- Sizing validation performed with built-in **test benches**, using **ngspice**.
- **Fast computation** to ease **interaction** with the designer.
- Input and output results available through a **GUI** and input/output files.
- Coupled with **Coriolis** layout engine.
- Distributed as Free/Libre and Open Source Software **FOSS**.
- Goal : **distributed** on top of **ngspice** ?

# Thank you for your attention !

<https://www-soc.lip6.fr/equipe-cian/logiciels/oceane/>