# From filters to transistors

## A library of analog schematic with automated sizing

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# Plan


1. Sizing and characterizing a MOS transistor
2. Sizing and characterizing a Miller amplifier
3. Sizing and characterizing an elliptic Filter
4. Conclusion

1 Sizing and characterizing a MOS transistor

2 Sizing and characterizing a Miller amplifier

3 Sizing and characterizing an elliptic Filter

4 Conclusion

# Analog Design : biasing, sizing and characterizing the MOS transistor

- MOS calculator

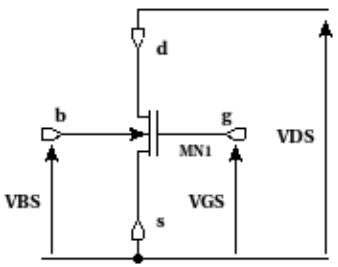
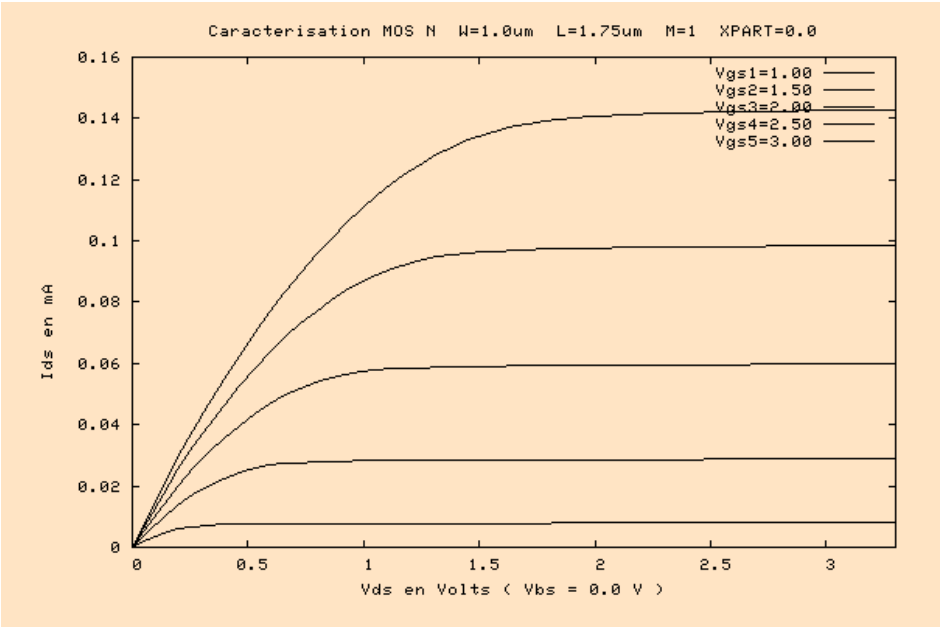



FIGURE: MOS transistor with its 4 terminals : gate, drain, source, bulk.

- MOS models (equations) : BSIM, ...
- + process parameters (foundry, technology nodes)
- analysis : $I_{DS}$ is computed
  $I_{DS} = f_{(model,process)}(W, L, V_{GS}, V_{DS}, V_{BS}, temp)$
- MOS regime :
  $V_{OV} = V_{GS} - V_{TH}$, overdrive voltage, inversion mode
  $V_{Dsat} = V_{GS} - V_{TH}$, saturation/linear
- sizing : $W$, $L$ or $V_{GS}$ are computed
  set $V_{OV}, W, L \Rightarrow I_{DS}, V_{GS}$
  set $V_{OV}, I_{DS}, L \Rightarrow W, V_{GS}$
  set $V_{OV}, I_{DS}, W \Rightarrow L, V_{GS}$

# MOS transistor calculator

Analyzing the MOS transistor : $I_{DS}(V_{DS})$ and $\frac{G_m}{I_{DS}}(V_{GS})$



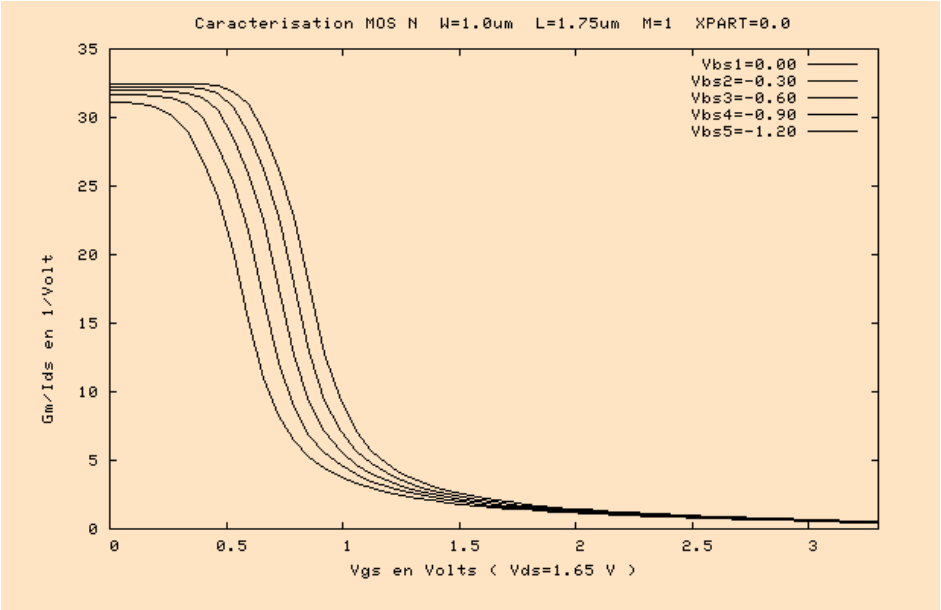




FIGURE: MOS transistor. Drain current $I_{DS}$ versus drain source voltage $V_{DS}$. $I_{DS} = f(W, L, V_{GS}, V_{DS}, V_{BS}, temp)$

FIGURE: $G_m$ over $I_{DS}$ versus $V_{GS}$, for various $V_{BS}$. Image of the overdrive voltage $(2/V_{OV})$.

# MOS transistor calculator

Sizing the transistor for the optimal overdrive voltage $V_{OV}$ :

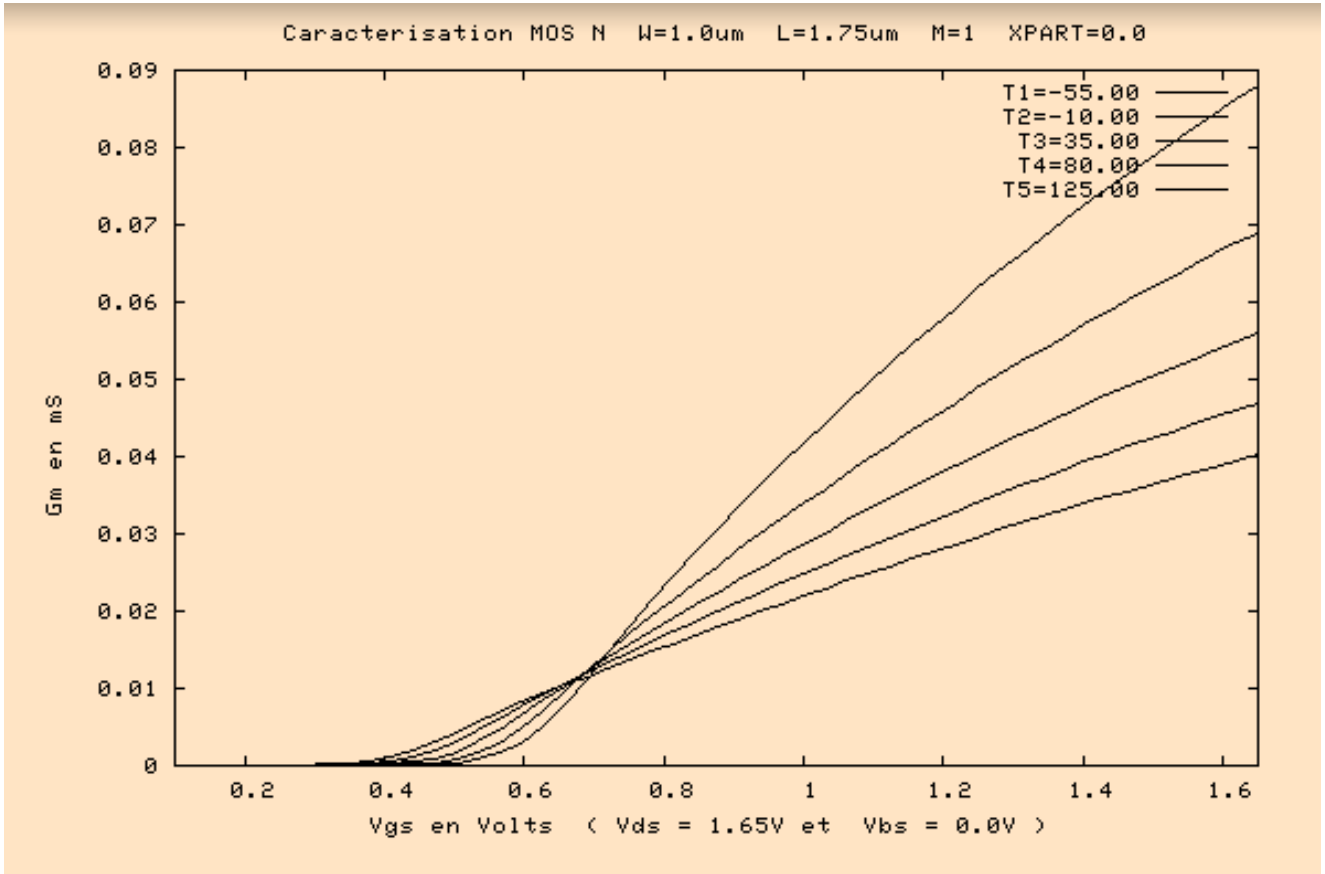



FIGURE: Transconductance Gm versus $V_{GS}$, for different temperatures in the range $[-55°C, 125°C]$. Selection of the optimal point : $V_{OV} \sim 0.2V$, according to temperature variation.

# MOS transistor calculator within Oceane

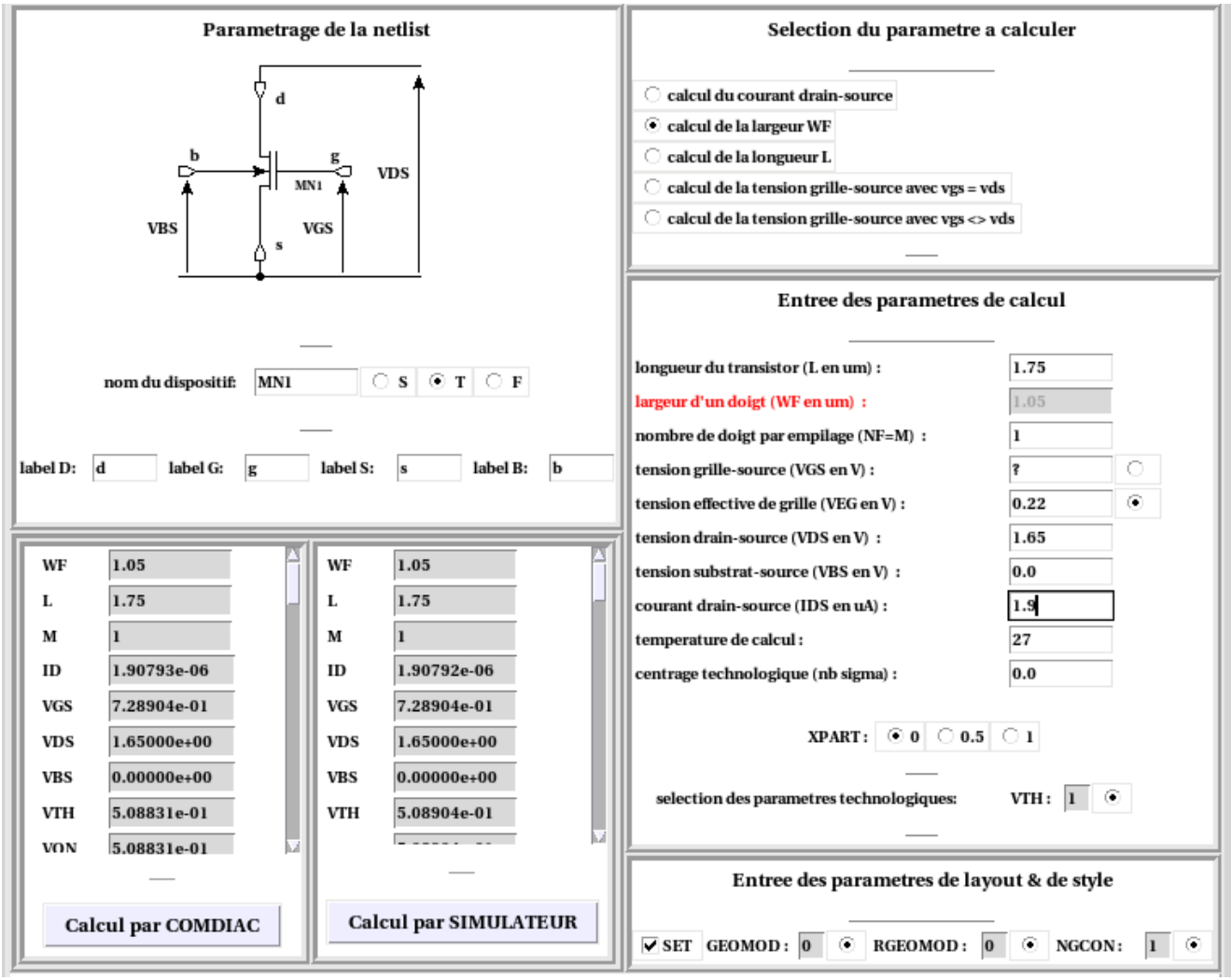



FIGURE: Oceane MOS transistor sizing (i.e. set $V_{OV}, I_{DS}, L \Rightarrow W, V_{GS}$) and characterizing cockpit. Oceane and **nspice** results are equal.

# Behind the MOS transistor cockpit

- Oceane/COMDIAC built-in MOS transistor models

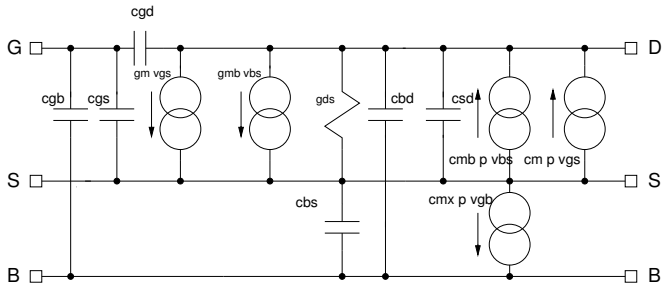



FIGURE: Small signal equivalent schematics.

- Complete MOS transistor model (as in simulator)
- Official parameters of the BSIM3/4 models (NDA)

- all parameters are taken into account :
  - layout dependent parameters
  - Stress effect
  - multi $V_{TH}$
- **ngspice** simulator is called to validate each design
- a library of configurable test benches is available
- DC operating point, transient analysis, and AC analysis can be performed.

1 Sizing and characterizing a MOS transistor

2 Sizing and characterizing a Miller amplifier

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4 Conclusion

# Analog Design : biasing, sizing and characterizing the Miller amplifier

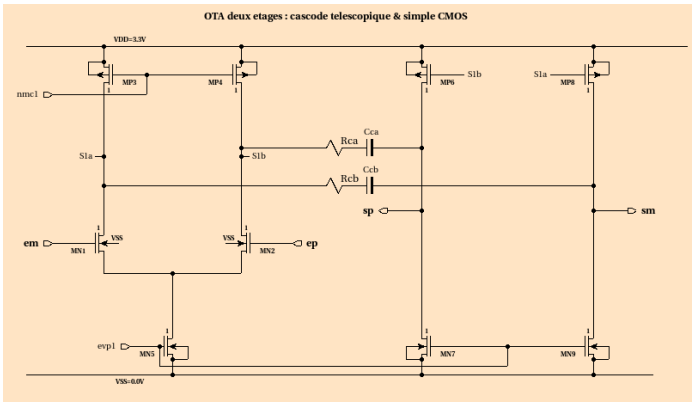


FIGURE: 2 stage Miller amplifier. Several topological alternatives are provided.

- Selection of topology, with several alternatives
  - Differential pair : NMOS/PMOS
  - Cascode
  - Compensation : C alone, R and C
  - Common mode rejection circuit for differential structures
  - ...
- Specifications (a small set)
- Computation (fast to be iterated)
  - Launched from GUI
  - or C file
  - $\Rightarrow$ W,L, R and C
- Computed performances (**Maxima**, building symbolic transfer functions)
- Simulated performances (validation)

# Sizing Principle : Amplifier case study.

1. level 1 MOS transistor model, used to illustrate the main steps : $I_{DS} = \frac{\mu}{2} C_{ox} \frac{W}{L} (V_{OV})^2 (1 + \lambda \cdot V_{DS})$, with $V_{OV} = (V_{GS} - V_{TH})$ (1)
2. Specification of the power $\Rightarrow I_{DS}$, the biasing current or Unity Gain Frequency : $F_U \sim \frac{g_m}{2\Pi C_L}$
3. The inversion level : $V_{OV} \Rightarrow g_m = \frac{2 I_{DS}}{V_{OV}}$, the transconductance
4. Gain specification : $A_{d0} \sim \frac{g_m}{g_{ds}} \sim \frac{L \cdot V_E}{V_{OV}} \Rightarrow L$ since $\lambda = \frac{1}{L \cdot V_E}$
5. Transistor sizes, computed from Eq. 1 (step 1)
6. Secondary performances : input thermal noise $\sim \frac{K \cdot Temp}{g_m}$, possible iteration (step 4)
7. Test benches for performance simulation ($\sim$ computed ones)

**Oceane**

Complete MOS transistor models are used instead of Eq. 1 in Step 1, so that a perfect matching between Oceane and **ngspice** is achieved.

# Analog Design : sizing the Miller amplifier

GUI with input and output files :

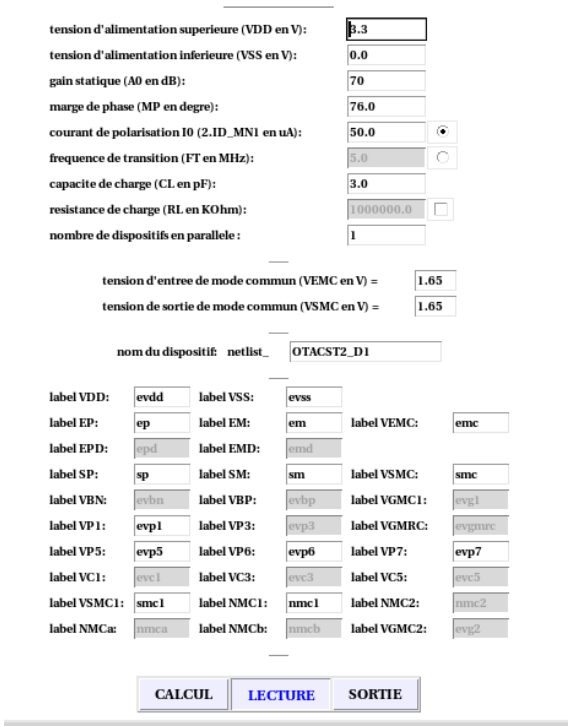


FIGURE: Millller amplifier specifications, input file

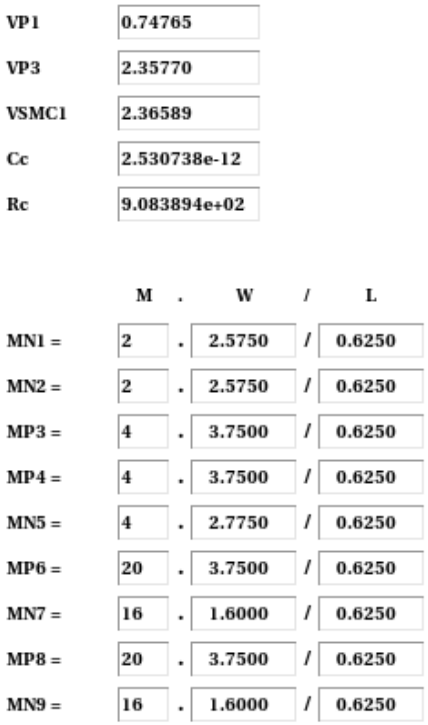


FIGURE: Millller amplifier MOS sizing, output file

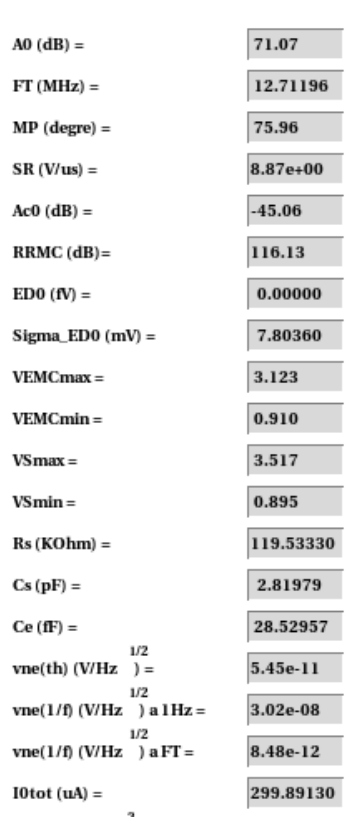


FIGURE: Millller amplifier performances, output file

# Validation of the Miller design with **ngspice** simulation

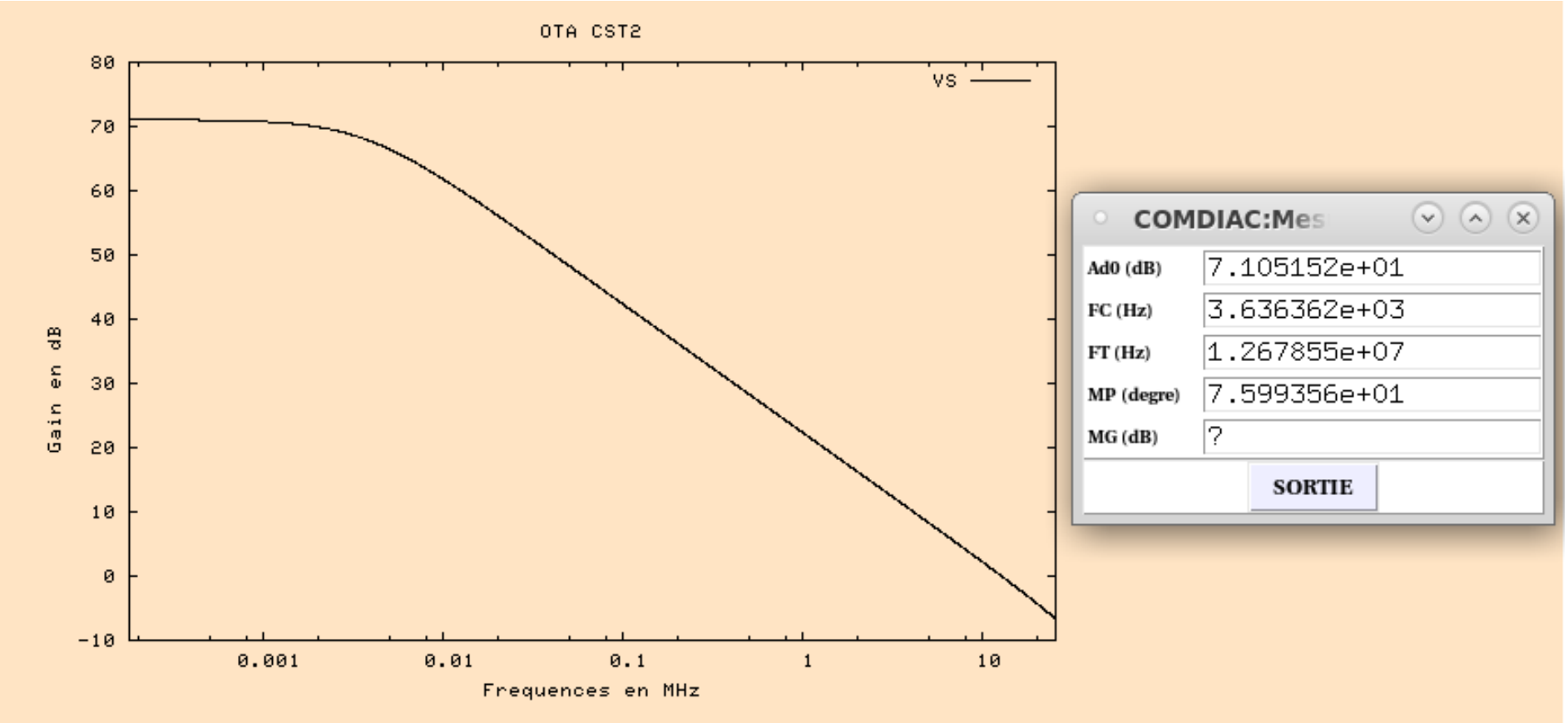


FIGURE: Gain (dB) versus frequency, **ngspice** simulation results, same as computed performances.

# Layout of the Miller design with **Coriolis**

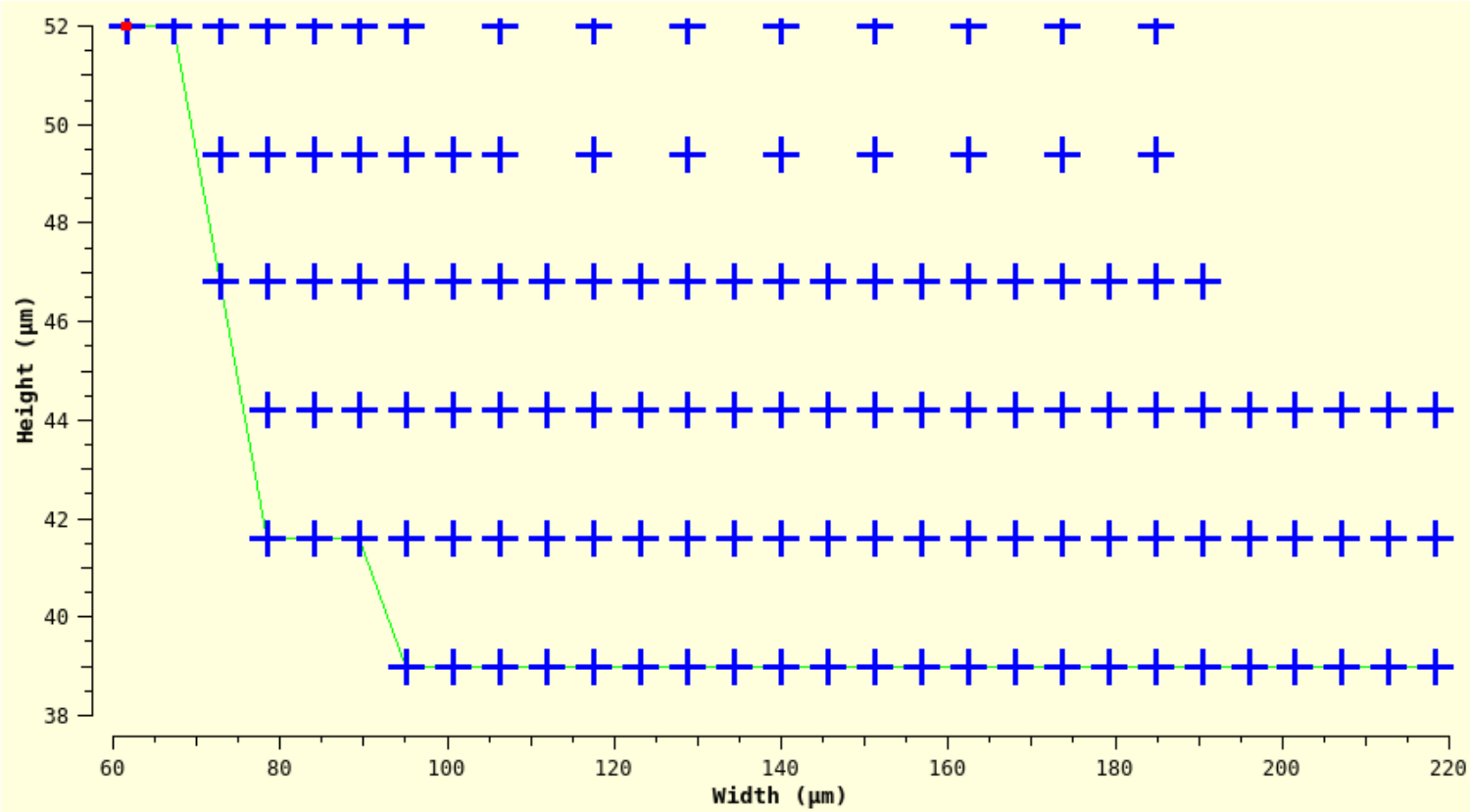


FIGURE: Shape Function, computed by varying the number of transistor folds, for each transistor, of a netlist sized with Oceane.

# Layout of the Miller design with **Coriolis**

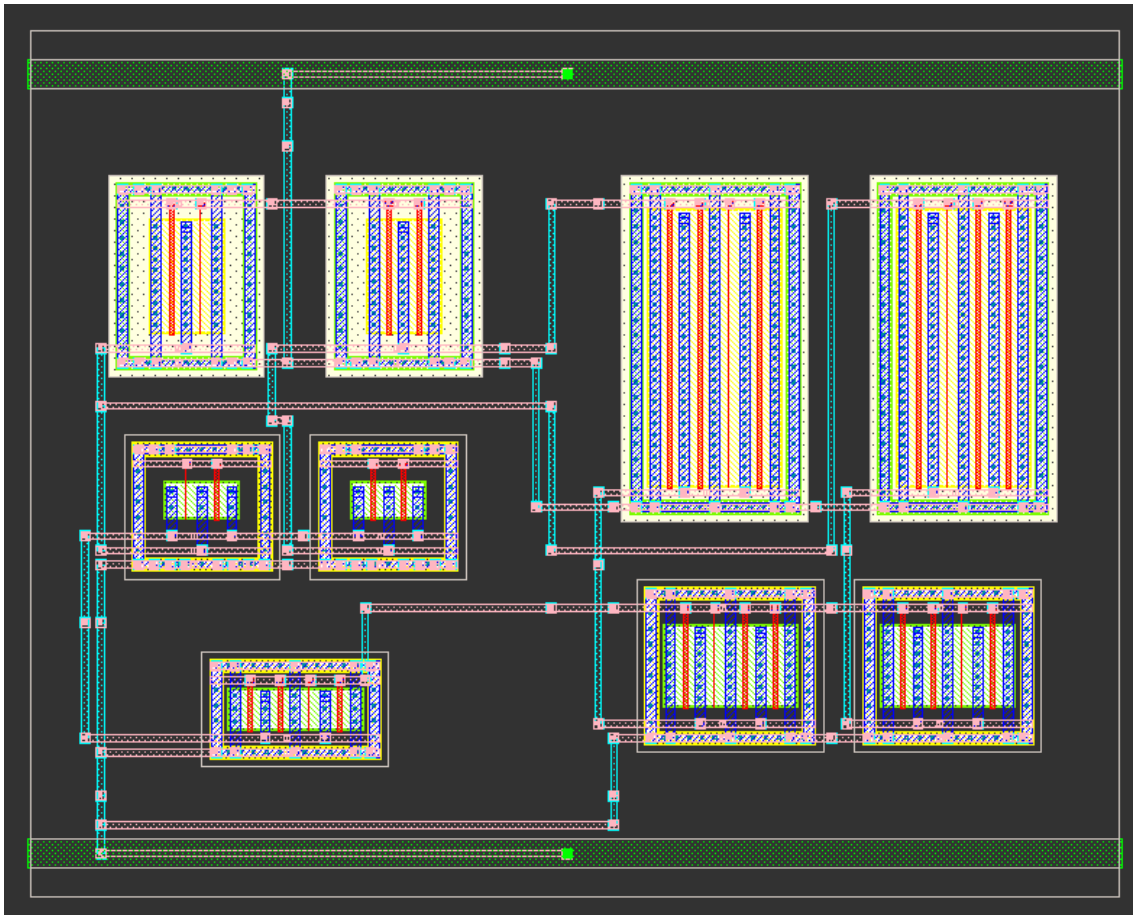

FIGURE: Layout of the square shape, transistor part, sized with Oceane.

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# Filter specification

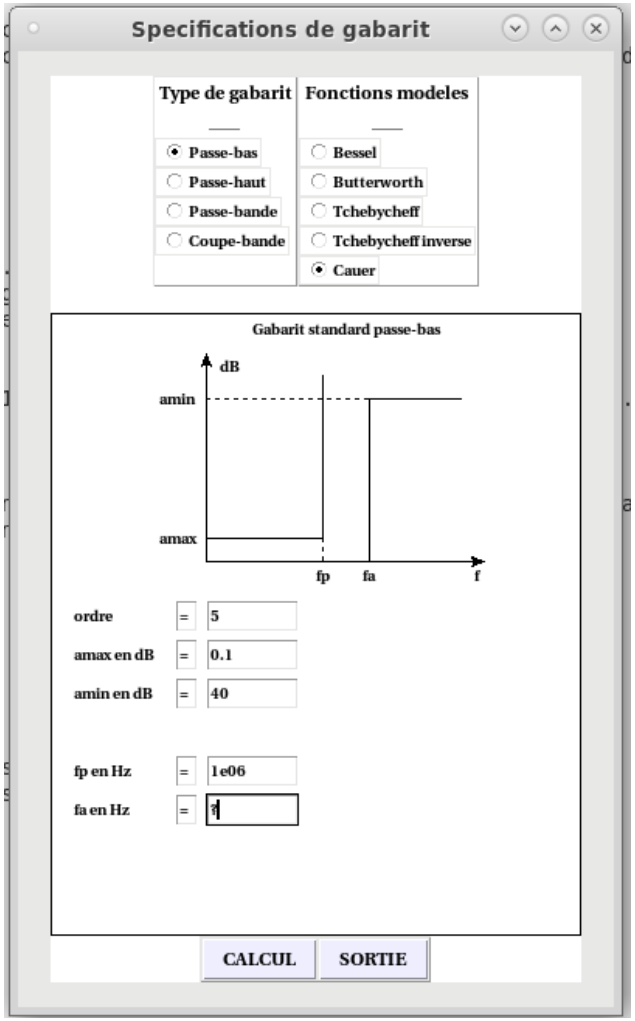


FIGURE: Filter specifications

- Type of filtering transfer function : Low-pass / band-pass / high-pass
- Specifications (a small set) :
  - Order of the transfer function (TF)
  - Frequency boundaries
  - Gain boundaries
  - Response shape :
    - ★ Chebyshev
    - ★ Butterworth
    - ★ Bessel
    - ★ Elliptic filter or Cauer filter

# Transfer function : Cauer, order 5

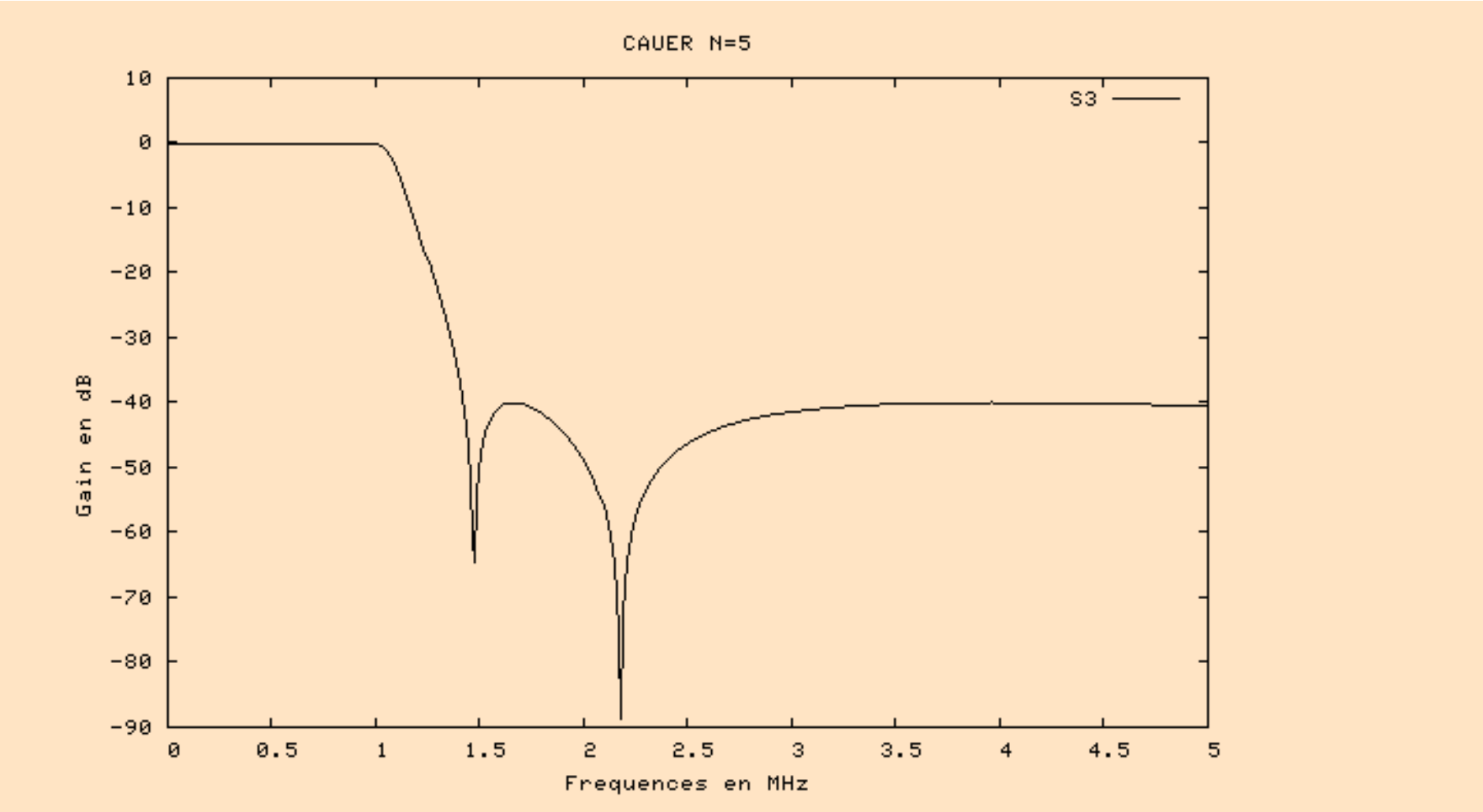


FIGURE: Transfer function of the filter : Gain (dB). Ideal models (OTA, R and C are used)

# Filter design : cascade of 1st order cell and 2 biquad cells

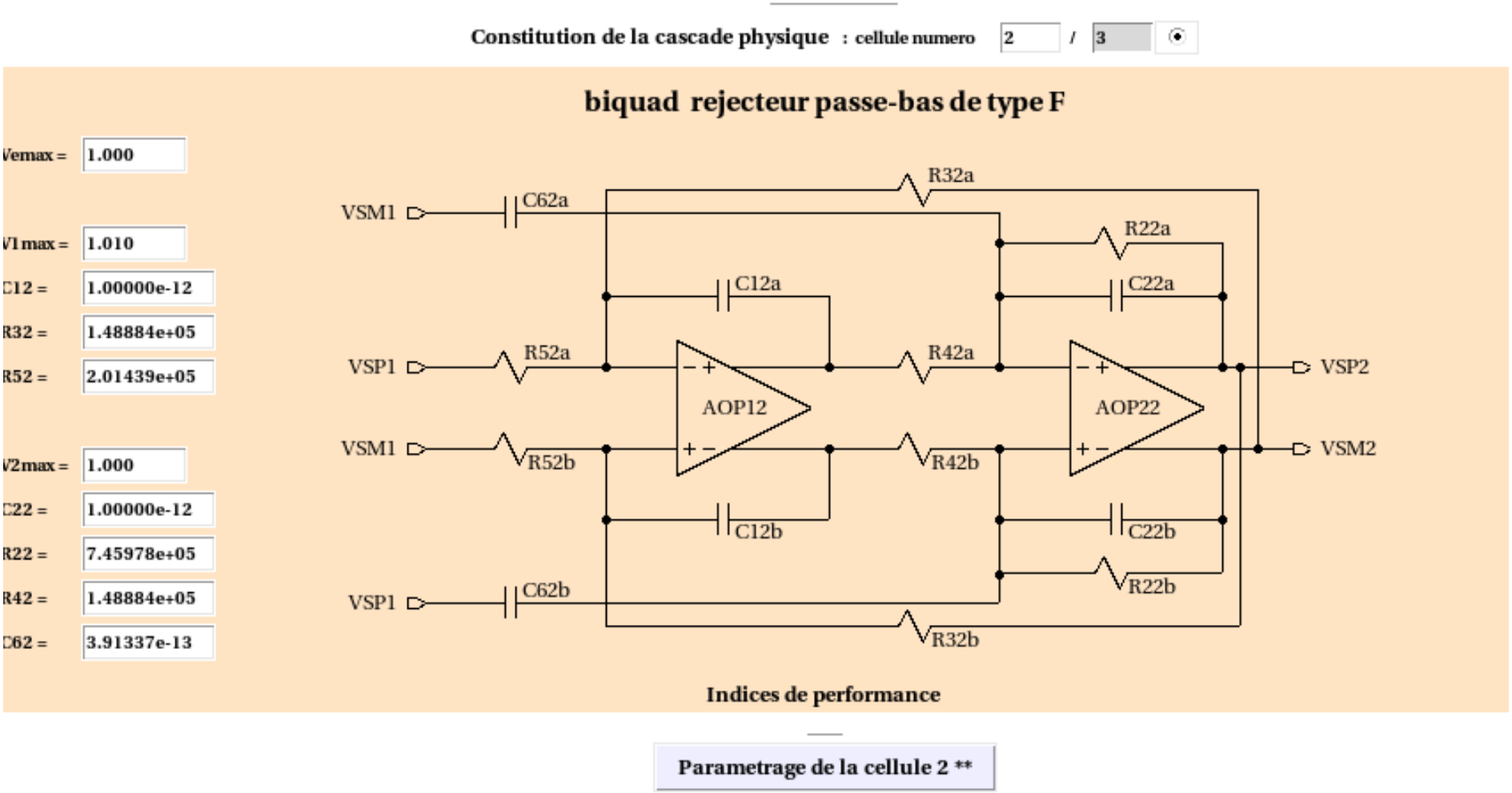


FIGURE: Second cell of the cascade (order 2)

# Filter design with 3 cascaded cells : amplifier specifications

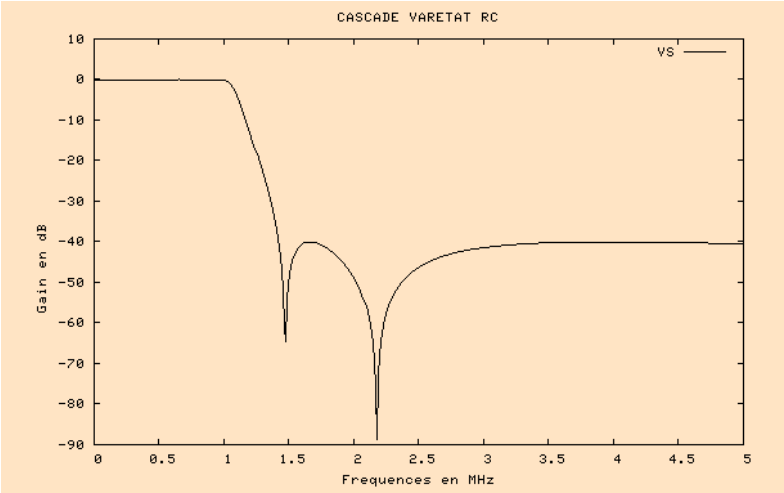


FIGURE: Transfer function of the filter : Gain (dB). Macromodels (OTA) are used with stringent specifications to fulfill the filter specifications ⇒ high power consumption.

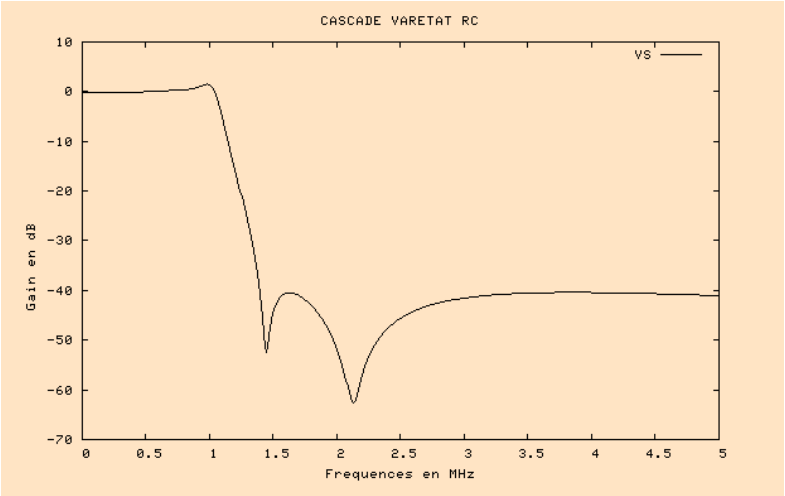


FIGURE: Transfer function of the filter : Gain (dB). Macromodels (OTA) are used with relaxed specifications to decrease the whole power consumption ⇒ Filter TF error.

# Filter design : cascade of biquad cells, optimization

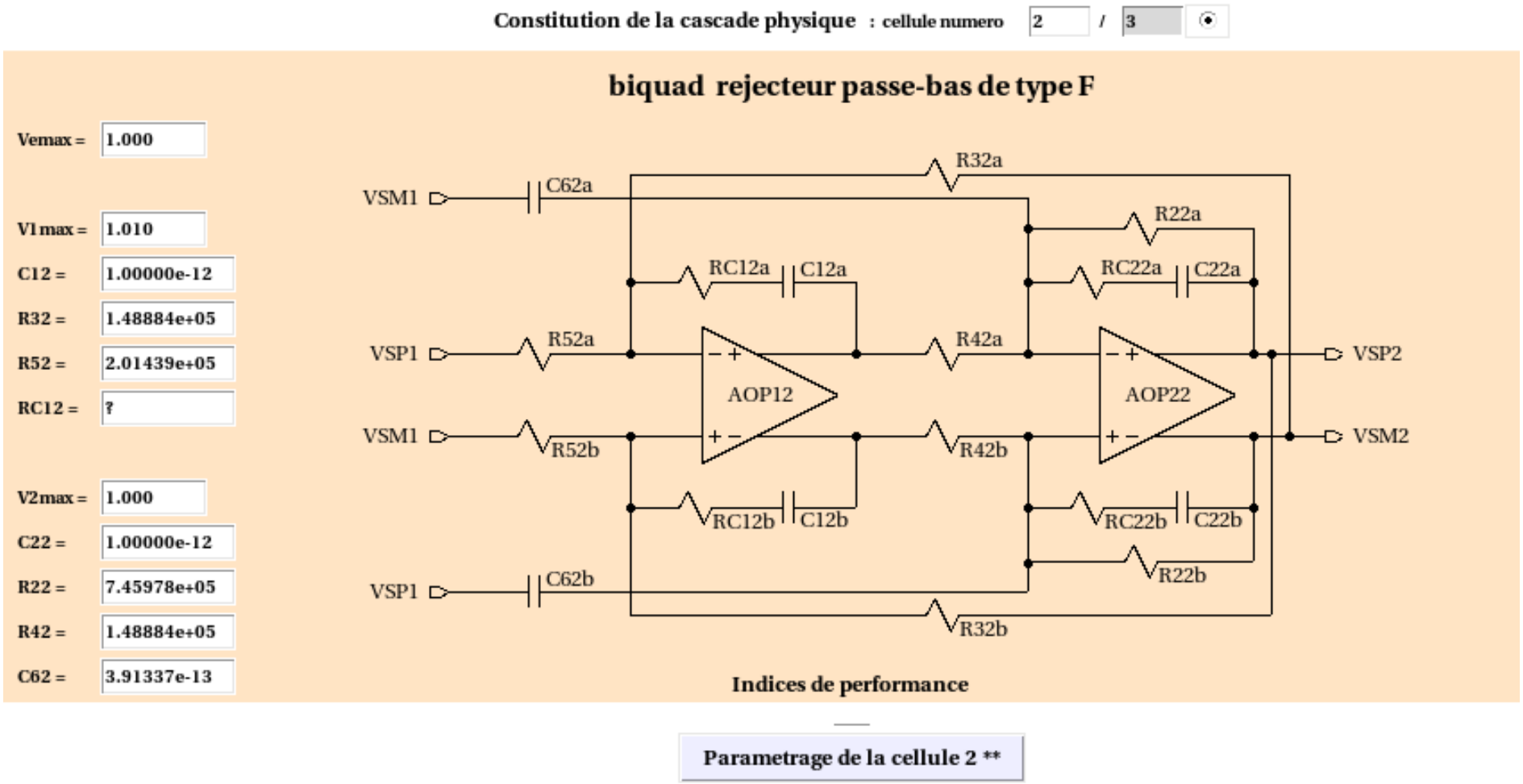


FIGURE: $2^{nd}$ cell of the cascade (order 2) modified to lower the filter power consumption. The low amplifier gain impact is corrected by resistors in series, (variant available).

# Transfer function : cascade of biquad cells, validation

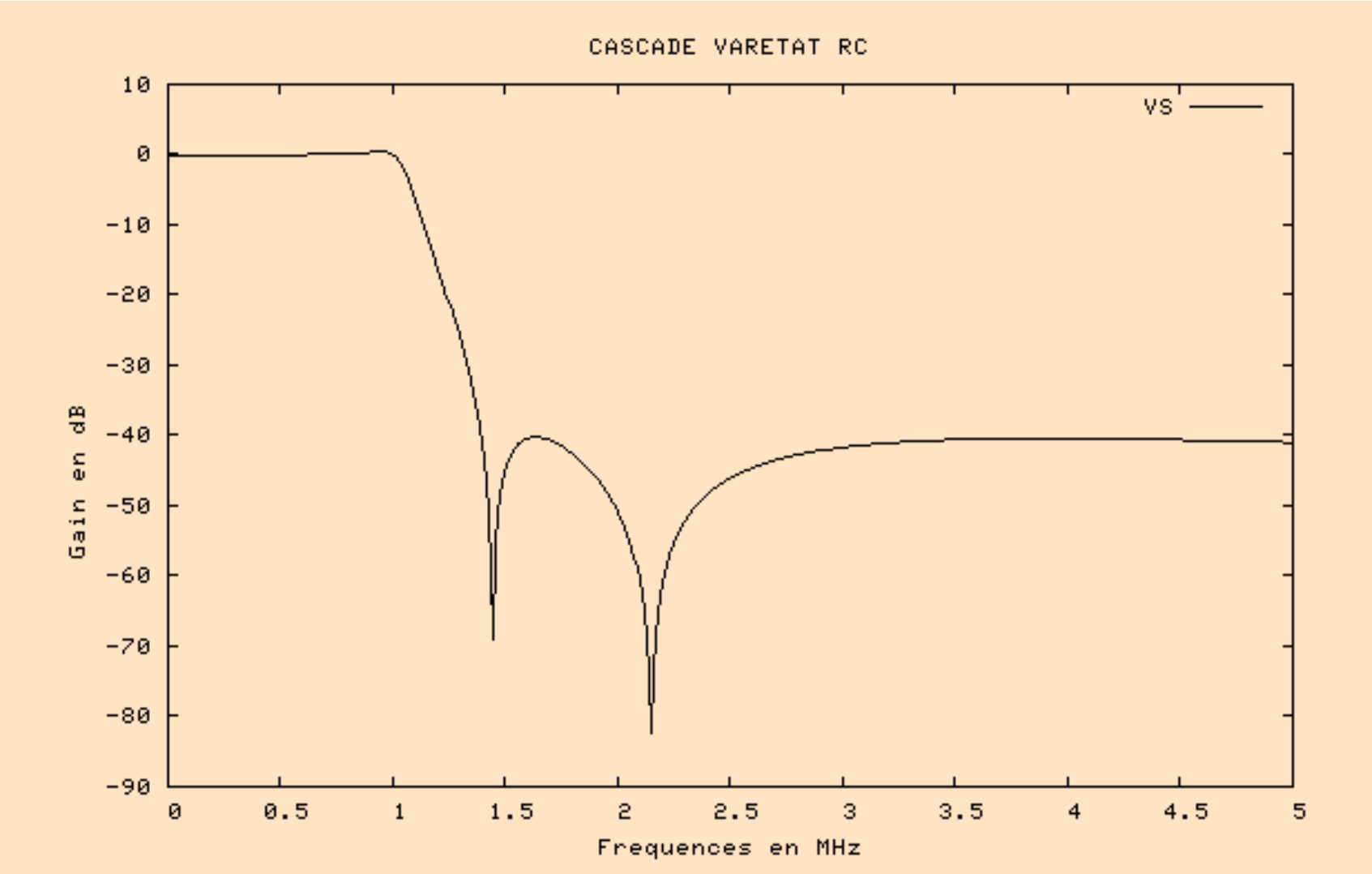


FIGURE: Validation by **ngspice** simulation (macro models of the amplifiers with relaxed specifications and correction) $\Rightarrow$ correction of the Filter TF.

# Filter : cascade of biquad cells, Miller amplifier at transistor level

## Transistor Level and symbolic computation

Complete MOS transistor models are taken into account to compute the symbolic TF of the filter, to achieve a perfect matching between Oceane computed performances and **ngspice** simulation.

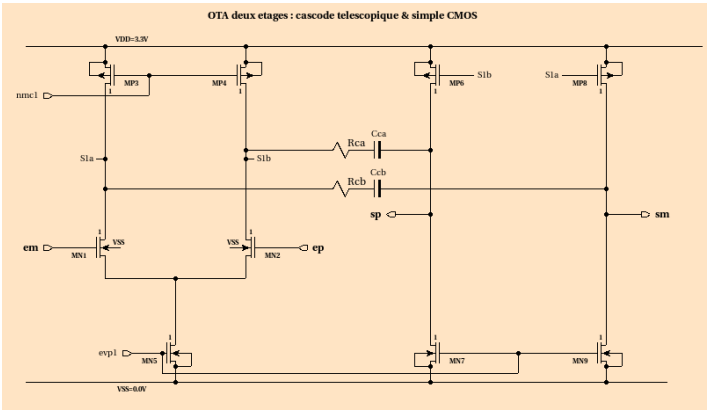


FIGURE: Millller amplifier, sized with specifications coming from the macro-model based biquad

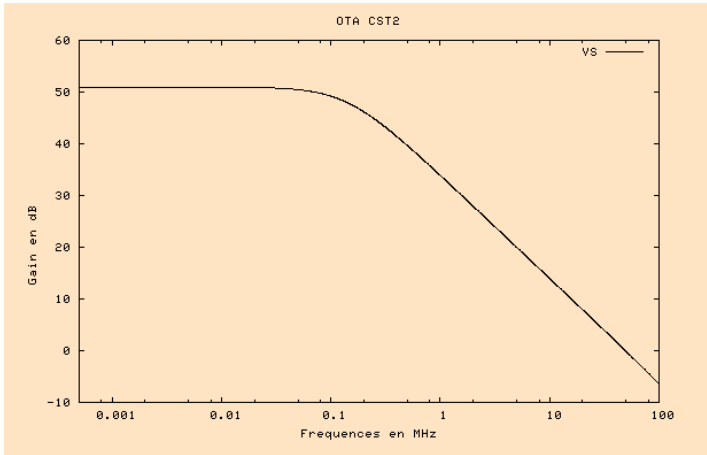


FIGURE: Millller amplifier gain

# Transfer function : cascade of biquad cells, transistor level

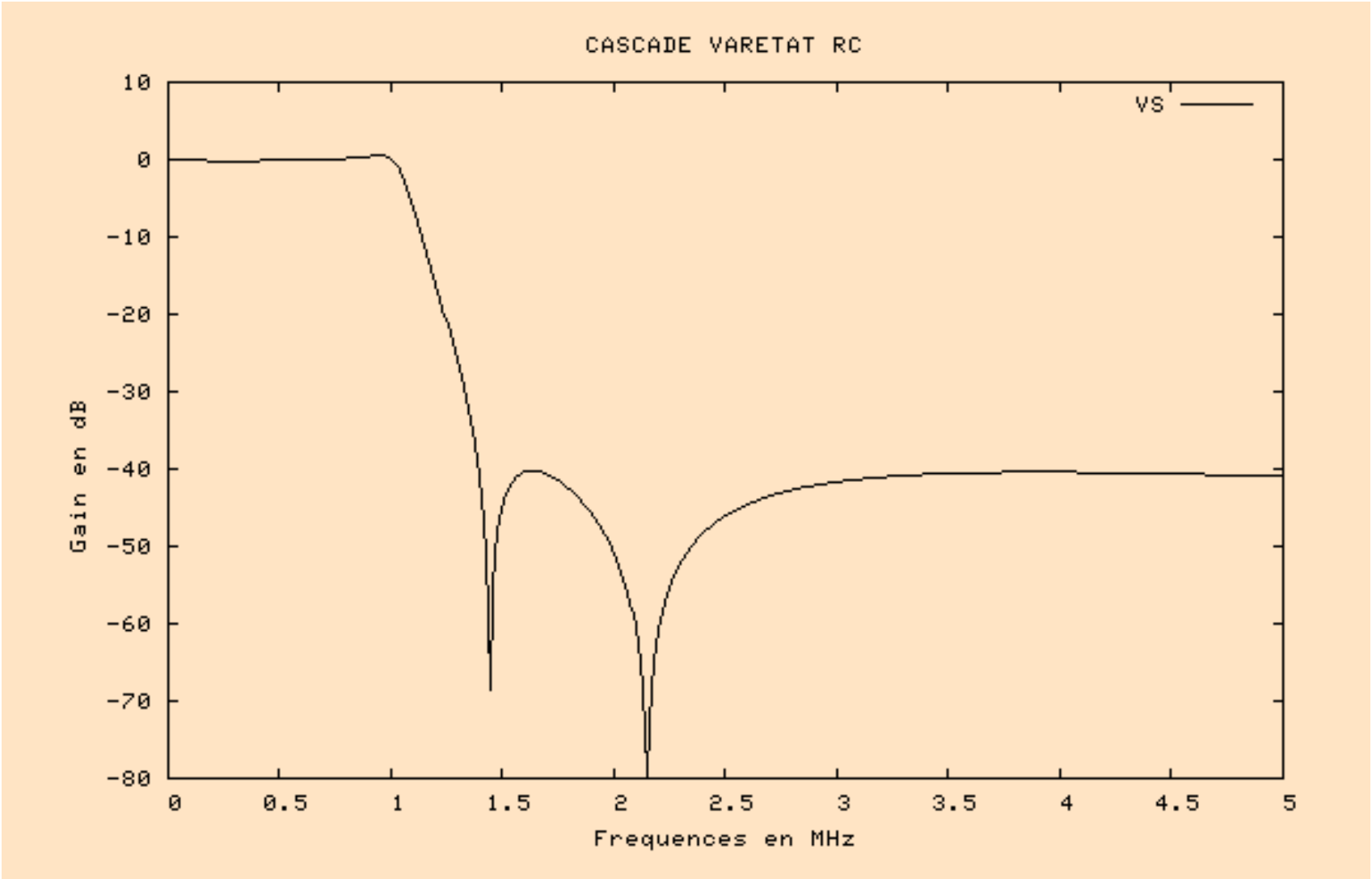


FIGURE: Validation by **ngspice** simulation (full transistor netlist.)

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# Oceane

- Filter design : from specifications to transistor netlist.
- Accurate sizing, based on the same complete MOS transistor model (BSIM3/4, ...) than the simulator, to ensure accurate sizing.
- Transistor sizing is based on the overdrive voltage (independent of the process to ensure technology migration).
- Sizing validation performed with built-in test benches, using **ngspice**.
- Fast computation to ease interaction with the designer.
- Input and output results available through a GUI and input/output files.
- Coupled with **Coriolis** layout engine.
- Distributed as Free/Libre and Open Source Software FOSS.
- Goal : distributed on top of **ngspice** ?

# Thank you for your attention !

https ://www-soc.lip6.fr/equipe-cian/logiciels/oceane/