



Towards Foundry PDKs on Free CAD Tools

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- **Introduction**
- **CMP Viewpoint on PDKs & CAD Tools**
- **Full-Custom Design Flow : What's needed ?**
- **Free CAD's PDK development at CMP**
- **Perspectives**



Introduction

- ❑ **CMP started in 1981 offering MPW runs for Universities / Research Labs. Long experience on CAD tools and PDK development, distribution and support.**

- ❑ **Free Layout Editors in the 80's :**
 - 1980 : **MAGIC** made by University of Berkeley and distributed by MOSIS, USA
 - 1984 : **LUCIE** made and distributed by CMP, France

- ❑ **CAD tools supported at CMP**
 - 1986 : University Program CAD distribution : CNFM, France
 - 1989 : University Program CAD distribution : Eurochip, then Europractice.
 - Till Today : CAD tools distributed by CNFM in France & Europractice in EU.
(CAD tools mainly from the big three : Cadence, Mentor, and Synopsys)

- ❑ **PDKs developments, distribution, and support at CMP**
 - 1990 : First Complete PDK for AMS 1.2 μ CMOS (Analog & Digital design-flows)
 - Several PDK developments made by CMP on commercial CAD tools.
 - Today : More than 20 different foundry's design-kits distributed and supported.

❑ PDK and CAD Tools :

- PDK : A set of files and configurations embedding Foundry's tech. data.
- CAD : Computer Engine assisting the design automation.

❑ PDK for a given CAD Tool :

- Foundry's Tech. data written in formats supported by the CAD tool.
- Need to be foundry certified.
- Need to be updated as CAD tools evolve.

❑ Free CAD Tool requirements for a viable Foundry's PDK :

- Foundry's tech. data could be translated into the Free CAD Tool Format.
- Support of standard CAD formats (GDSII, Spice, Verilog, Oasis, LEF, DEF, CDL, ...)
- Foundry reference flow could be implemented.
- Passing benchmarks similar to the Foundry's reference PDK.
- Having a continuous updates and support.

Free front-end CAD Tools :

- Schematic entry / Spice simulation tools widely available:

Xcircuit, ngspice, Spice3f5, SpiceOpus, gEDA, LTSpice, Alliance, etc ...

Free backend CAD Tools :

- Several Freeware layout tools are available: Magic, Electric, Klayout, LayoutEditor, Toped, Electric, Glade, Alliance, etc ...

Front-End

Schematic Entry

Spice Simulation

Layout Edition

DRC

LVS

Layout Parasitics
Extraction

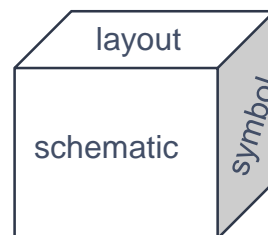
Post-Layout
Simulation

GDSII tape-out

BackEnd

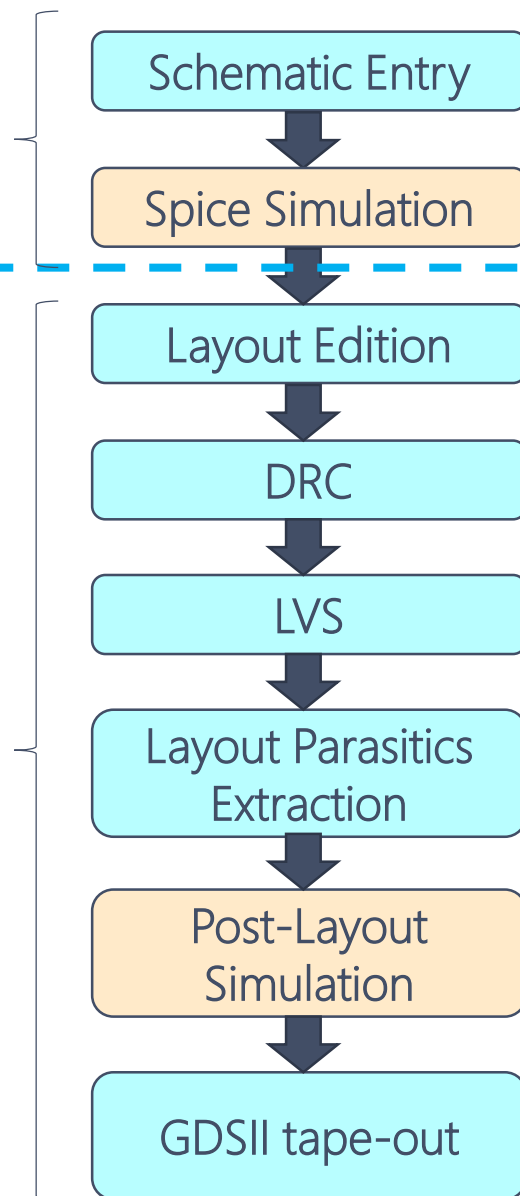
❑ Glade : <http://www.peardrop.co.uk>

- Support of Linux, Windows & Mac.
- Support of standard CAD formats : GDSII, Oasis, CDL, EDIF, Verilog, LEF, DEF, etc ...
- Support of Python programming language.
- Unified cellview concept :
 - layout, schematic, symbol, netlist, extracted



❑ Spice3f5 or SpiceOpus :

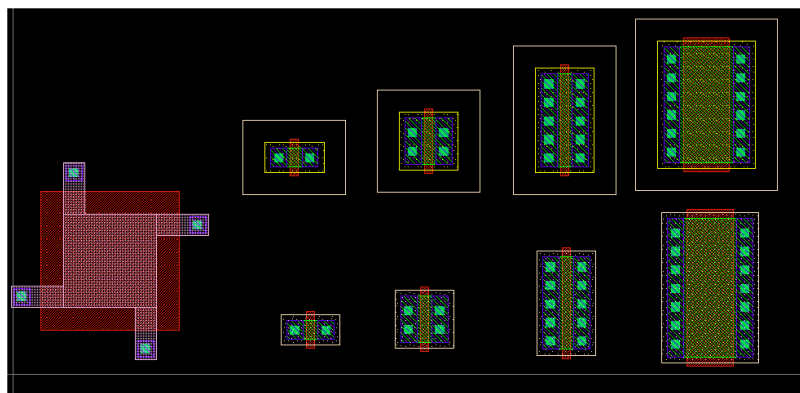
- Running from the Spice netlist output from Glade.
- Include waveform viewer.
- SpiceOpus Supports standard models : BSIM3, BSIM4, BSIMSOI, EKV, etc ...
- Run on Linux and Windows.





Glade PDK on 0.35 μ CMOS

- ❑ **Tech library** : Layer names, GDSII numbers, design rules, Via rules, colors and stipples, multi-parts paths, etc ... exactly the same as the foundry reference PDK (Cadence Virtuoso).
- ❑ **Pcells** : Same as the reference PDK.
- ❑ **Schematic entry** : Same as the reference PDK.
- ❑ **Schematic driven Layout.**
- ❑ **DRC** : about 90% implemented
- ❑ **Extraction & LVS for all devices**
- ❑ **2D LPE (Layout Parasitics extraction)**



LSW	
Edit	Display
NS	NV AS AV
M1	R1 M2 R2
NTUB	dwg
DIFF	dwg
NPLUS	dwg
PPLUS	dwg
MIDOX	dwg
HRES	dwg
POLY1	dwg
POLY1	pin
POLY2	dwg
POLY2	pin
CONT	dwg
MET1	dwg
MET1	pin
VIA1	dwg
MET2	dwg
MET2	pin
VIA2	dwg
VIA2	pin
MET3	dwg
MET3	pin
VIA3	dwg
MET4	dwg
MET4	pin
PAD	dwg
PIN	pol
PIN	met
PIN	met
PIN	met
PIN	met
PIN	pad
DIODE	dwg
METRES	met
METRES	met
METRES	met
METRES	met
SUBDEF	dwg
CELBOX	dwg
FIMP	dwg
METCAP	dwg
NLDD	dwg
NLDD50	dwg
RESDEF	dwg
RESTRM	dwg
TUBDEF	dwg
ZENER	dwg
SFCDEF	dwg

Glade Main Overview



Library Browser

Layers Selection Window

Menu Bar

ToolBar

Lib Names

Cell Names

View Names

The screenshot displays the Glade software interface with several components labeled:

- Library Browser:** A tree view on the left showing a hierarchy of libraries and components. It includes sections for 'Libs', 'Lib Names', 'Cell Names', and 'View Names'. The 'A_TEST' library is expanded, showing various components like 'BUF2', 'a_test_DRC', 'a_test_EXTR', 'a_test_LVS', 'a_test_sdl', 'all_devices', 'buffer', 'cpoly', 'cpoly_ex', 'inv', 'lat2', 'nmos', 'nmos4', 'padding', 'pmos4', 'rpoly1', 'rpoly1_ex', 'rpoly2', 'rpoly2_ex', 'rpolyh', 'rpolyh_ex', 'test_DRC', 'vert10_4', 'IOLIB 4M', 'PRIMLIB', 'a_D1', 'basic', and 'example'.
- Layers Selection Window (LSW):** A table in the center-left showing a list of layers and their types. The table has columns for 'Edit' and 'Display'. The layers listed include: NTUB (dwg), DIFF (dwg), NPLUS (dwg), PPLUS (dwg), MIDOX (dwg), HRES (dwg), POLY1 (dwg), POLY1 (pin), POLY2 (dwg), POLY2 (pin), CONT (dwg), MET1 (dwg), MET1 (pin), VIA1 (dwg), MET2 (dwg), MET2 (pin), VIA2 (dwg), MET3 (dwg), MET3 (pin), VIA3 (dwg), MET4 (dwg), MET4 (pin), PAD (dwg), PIN (pol), PIN (met), PIN (met), PIN (met), PIN (met), PIN (pad), DIODE (dwg), and METRES (met).
- Menu Bar:** Located at the top, containing 'File', 'View', 'Edit', 'Create', 'Verify', 'Tools', 'Window', and 'Help'.
- ToolBar:** A row of icons below the menu bar for various functions like opening files, saving, undo, redo, and zooming.
- Command Line:** A text input field at the bottom left for entering commands.
- Message Window:** A text area at the bottom right displaying the output of commands. The visible text is:

```
>>> ui().zoomIn(-35826, -5021, 24382, 26147)
>>> ui().selectPoint(150, 230, 0)
>>> ui().selectArea(333, 195, 401, 197, 0)
>>> ui().winFit()
>>> ui().winZoomOut()
>>> ui().zoomIn(-35225, -7740, 25608, 26725)
>>> ui().zoomIn(-33107, -6013, 23837, 25868)
>>> ui().zoomIn(-38, -74, 316, 352)
>>>
```
- Diagram Windows:** Two windows on the right showing the schematic and layout. The schematic window shows a circuit diagram with components like resistors, capacitors, and diodes. The layout window shows the physical layout of the components on a grid.

Command Line

Message Window

- ❑ **Complete full-custom design flow compatible with the foundry's reference flow.**

- ❑ **Need Foundry agreements to officially support Free CAD PDKs :**
 - **CMP in discussion with some.**

- ❑ **Define some policies and rules for supporting such tools.**
 - **Comercial tools still remain the reference.**
 - **Free CAD PDKs are not a replacement. They need to be a complementary offer helping in some situations (SMEs, ...)**
 - **Free CAD Tools could be used freely, while PDKs are subject to NDA.**

- ❑ **Next planned PDKs : 0.18 μ , 130nm CMOS. (in discussion with the foundries).**