Analyzing Open-Source Chip Design Ecosystem from an Environmental Sustainability Perspective

Prof. David Bol and ECS group

ECS group, ICTEAM institute, UCLouvain

david.bol@uclouvain.be

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UNION EUROPEENNE
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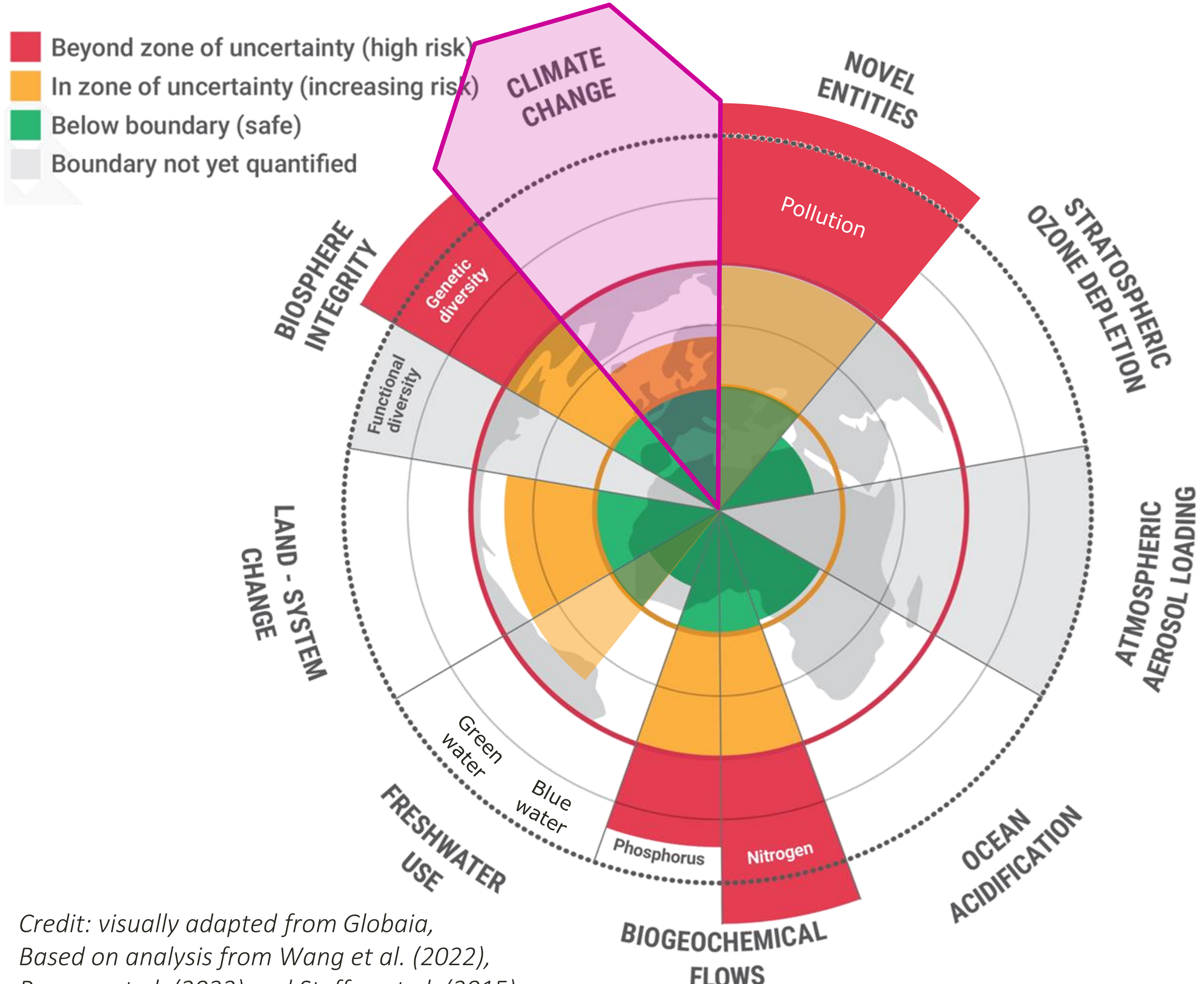
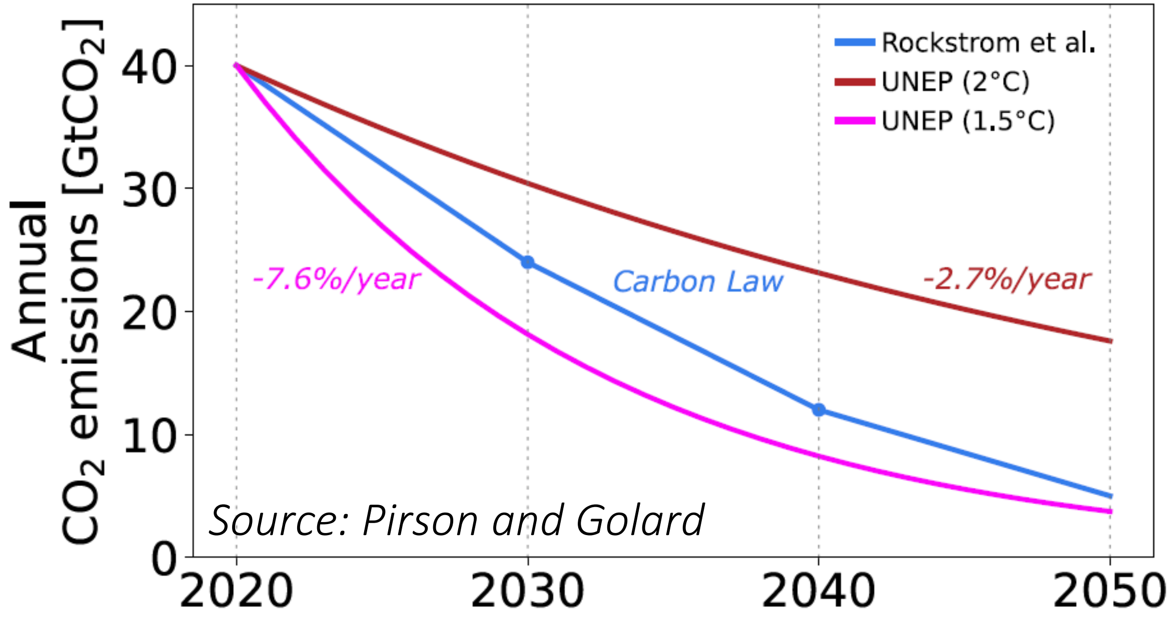
LE FONDS EUROPÉEN DE DÉVELOPPEMENT RÉGIONAL
ET LA WALLONIE INVESTISSENT DANS VOTRE AVENIR

PLANETARY BOUNDARIES
A safe operating space for humanity

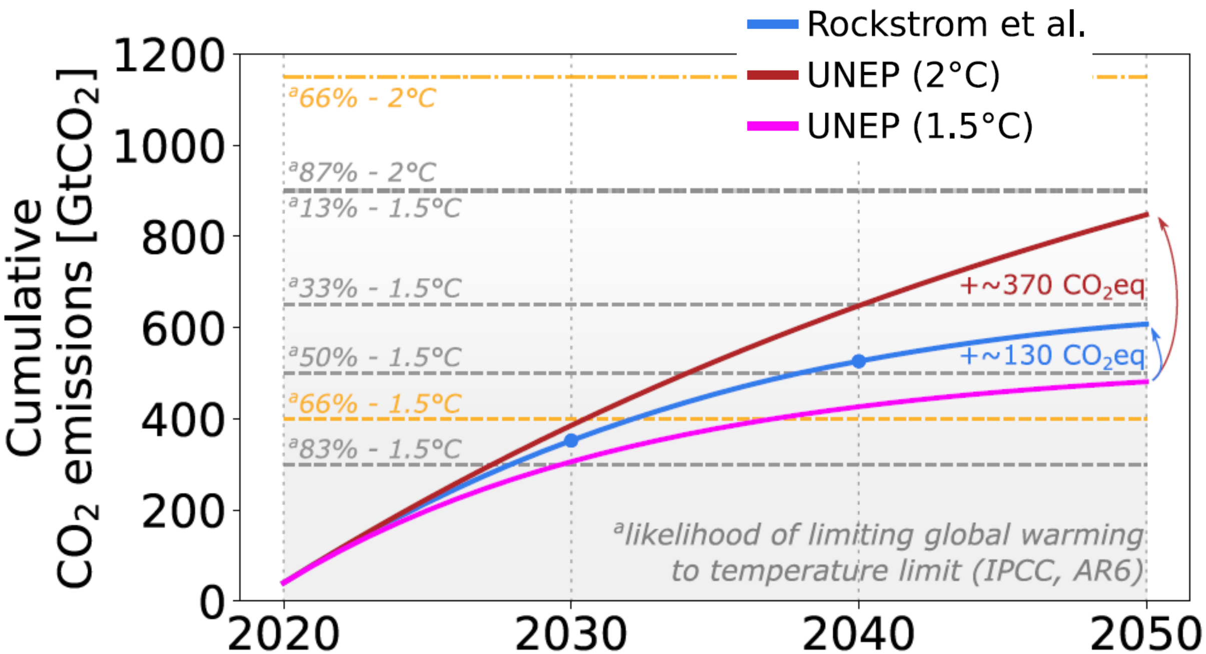


Credit: visually adapted from Globaia,
Based on analysis from Wang et al. (2022),
Persson et al. (2022) and Steffen et al. (2015)

Carbon budget



ICT accounts
for 2-4%
of global
GHG emissions
[Freitag et al., Patterns, 2021]



Outline

- Context: exceeded planetary boundaries
- Should the ICT carbon footprint be reduced?
- Moore’s Law and the global ICT energy demand
- Open-source chip design ecosystem
- How could we change course ?

Can we offset the GHG emissions of the ICT sector by avoiding emissions in other sectors ?

Avoided GHG emissions

- The claims for ICT:
  - *The 10:1 ratio [GSMA, The enablement effect]*
    One tonne of CO_2e emitted by the mobile sector would avoid 10 tonnes of CO_2e in other sectors.
  - *The 15-20% GHG reduction [GeSI, SMARTer2030]*
    Digitalization could reduce emissions in other sectors by up to 20% by 2030.

Avoided GHG emissions

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    One tonne of CO_2e emitted by the mobile sector would avoid 10 tonnes of CO_2e in other sectors.
  - *The 15-20% GHG reduction [GeSI, SMARTer2030]*
    Digitalization could reduce emissions in other sectors by up to 20% by 2030.

- Limitations of these studies:
  - Potential economic bias of the authors
  - Lack of transparency on the hypothesis & baseline
  - Disconnection from existing global scenarios for climate change mitigation
  - Limited scope: only positive “enabling” impacts are studied

[A. Rasoldier, et al., « How realistic are claims about the benefits of using digital technologies for GHG emissions mitigation? », in LIMITS, 2022]

Prof. Lorenz Hilty

Framework for the analysis of digital environmental impacts

Disclaimers:
- It neglects the indirect impacts of prod. & EoL
- The prob/sol normative positioning is too restrictive

	Digital / ICT as part of the problem	Digital / ICT as part of the solution	
Technology	Life cycle of ICTs: Production; Utilization; End of life (EoL)	(Not applicable)	1. Direct life-cycle impacts

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Application		Substitution, Optimization	2. Indirect « enabling » impacts

GeSI, GSMA

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GeSI, GSMA

Comprehensive and accurate accounting is not possible

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"LES" framework for the analysis of digital environmental impacts

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Technology	Life cycle of ICTs: Production; Utilization; End of life	(Not applicable)	1. Direct life-cycle impacts
Application	Induction; Obsolescence	Substitution; Optimization	2. Indirect « enabling » impacts
Socio-technical system	Rebound effect; Economy-wide transformation; Society-wide transformation		3. Indirect « structural » impacts

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Speculative

"LES" framework for the analysis of digital environmental impacts

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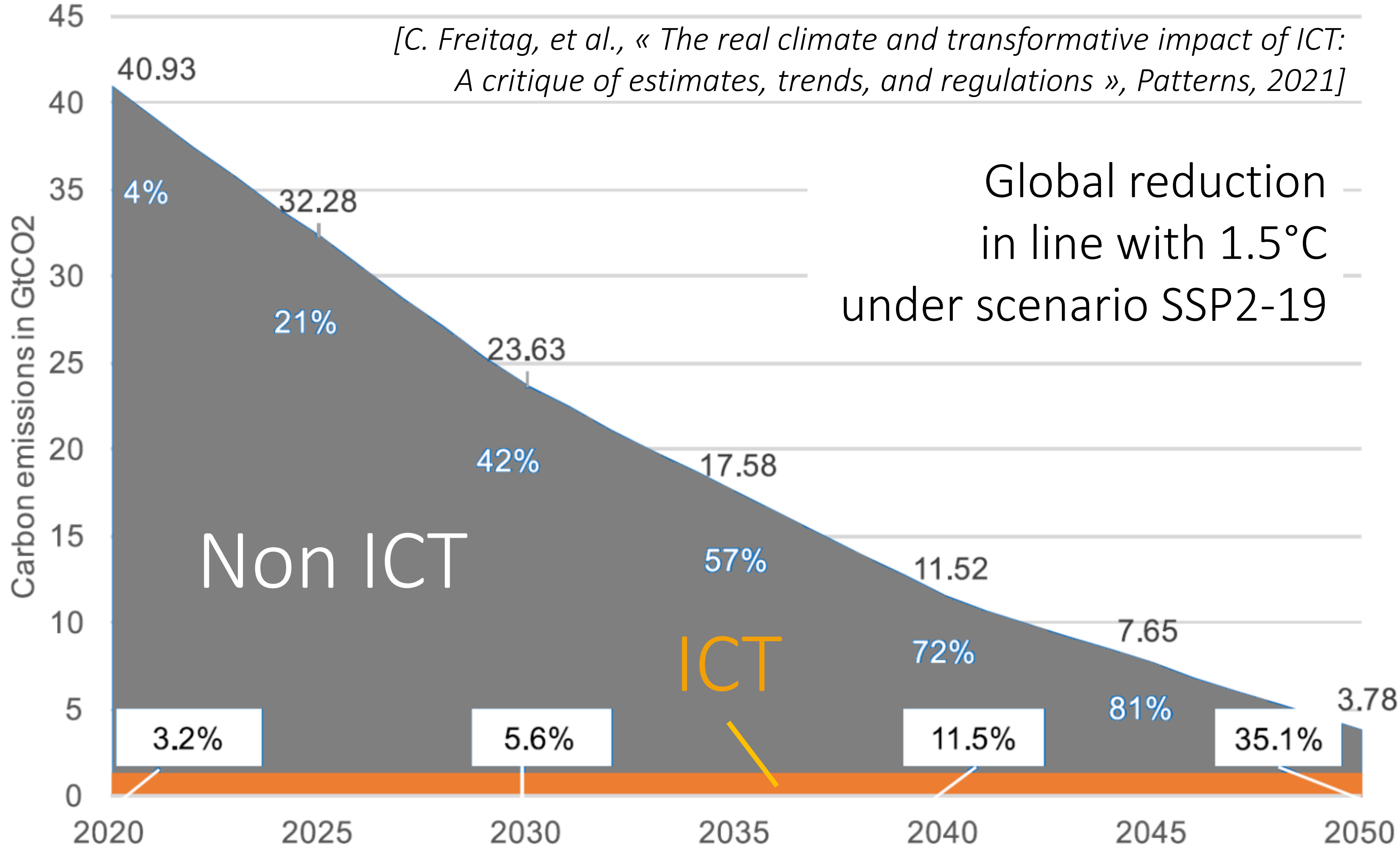
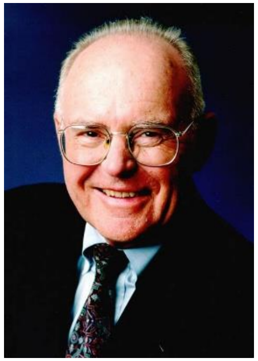
	Digital / ICT as part of the problem	Digital / ICT as part of the solution	
Technology	Life cycle of ICTs: Production, Utilization, End of life **GHG must go down by 7.6%/year (UNEP 1.5°C)**	(Not applicable)	1. Direct life-cycle impacts
Application	Induction Obsolescence **Comprehensive and accurate accounting is not possible**	Substitution Optimization	2. Indirect « enabling » impacts
Socio-technical system	Rebound effect Economy-wide transformation Society-wide transformation **Speculative**		3. Indirect « structural » impacts

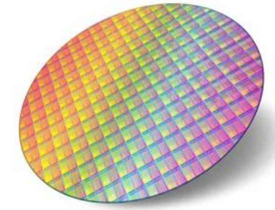
GHG reductions with a stable ICT footprint

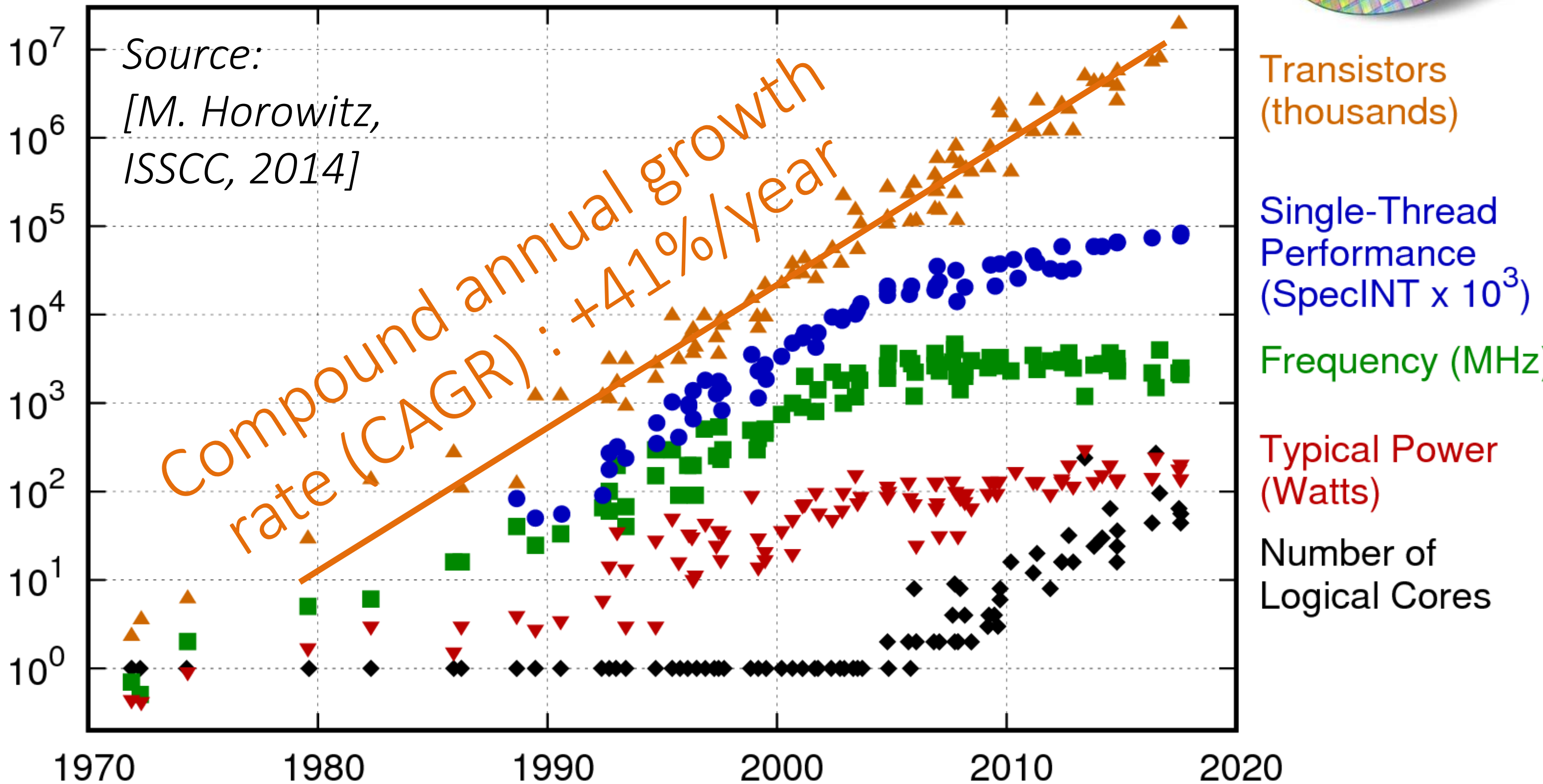


Moore's Law and the pursuit of efficiency cause an increase of the energy demand (lock-in situation in ICT)

Moore's law



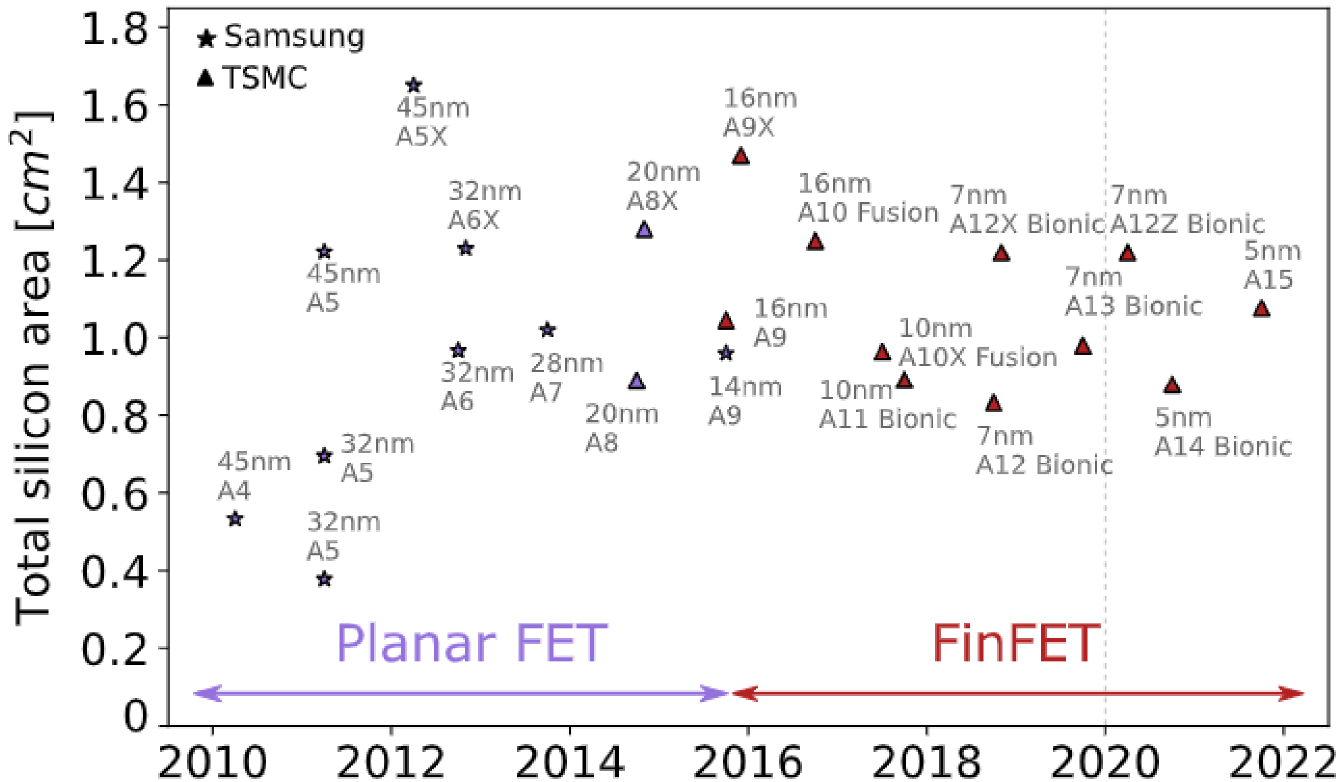




"The number of transistors per chip is doubling every 2 years"

Tech. scaling = higher silicon efficiency

Are chip getting smaller ?

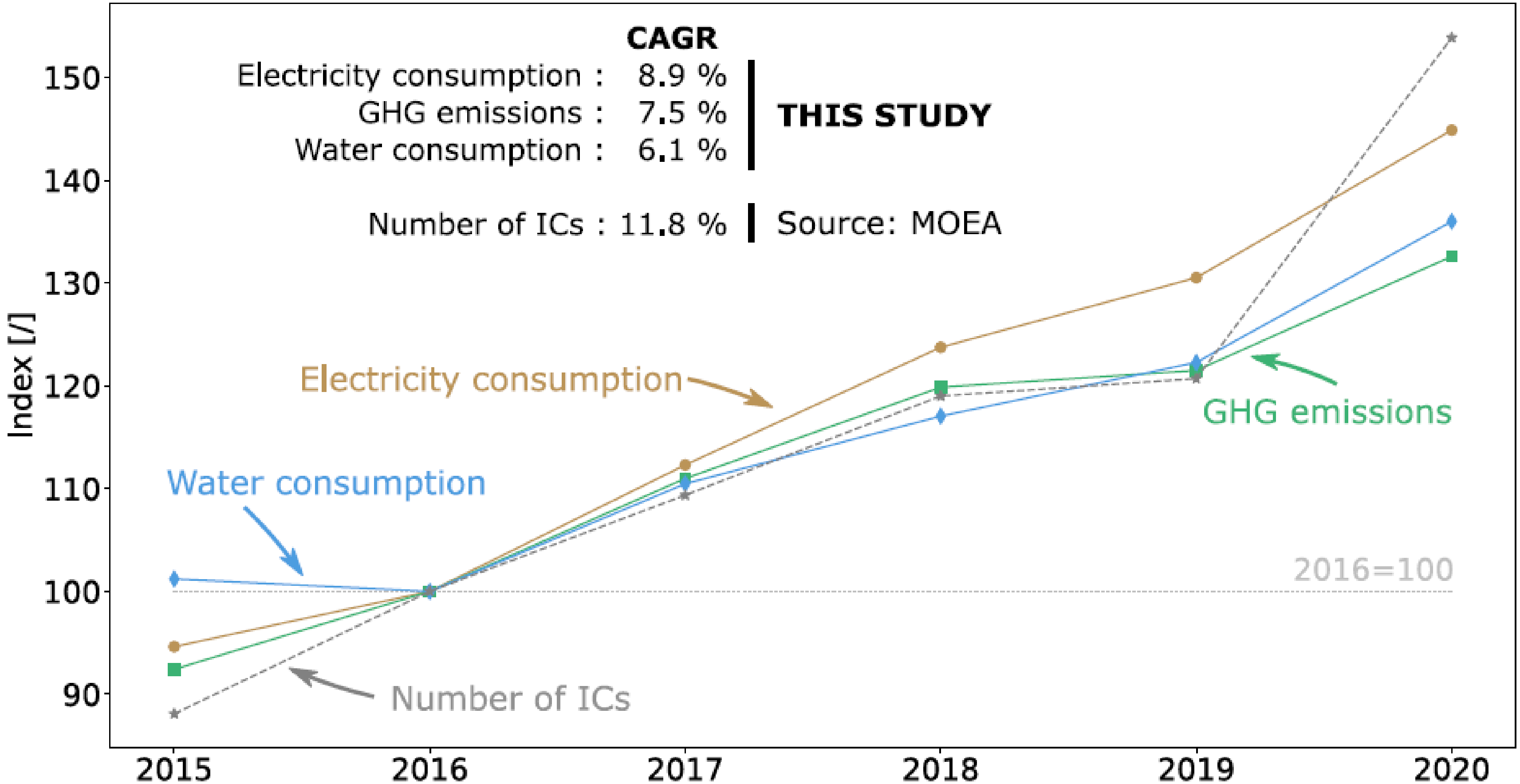


Application processors from Apple in iPhones

Typical chip products are not getting smaller with CMOS technology scaling despite the increasing transistor density

[T. Pirson, D. Bol, et al., « The Environmental Footprint of IC Production: Meta-Analysis and Historical Trends », in IEEE ESSDERC, 2022]

Evolution of the environmental impacts (production of electronic components)



[G. Rousshile, T. Pirson, D. Bol, et al., « From Silicon Shield to Carbon Lock-in? The Environmental Footprint of Electronic Components Manufacturing in Taiwan (2015-2020) », arXiv pre-print, 2022]

Cooper’s law

M. Cooper (ex. Motorola, founder of Arraycom) demonstrated the first cellular phone call on April 3, 1973 with the Motorola DynaTAC
→ 1.1 kg, 35-minute talk time

(“longer than you can hold the phone”)

Cooper's law

Since 1900, wireless communication capacity has doubled every 2.5 year

Compound annual growth rate (CAGR): +31%/year

More complex modulation = higher efficiency

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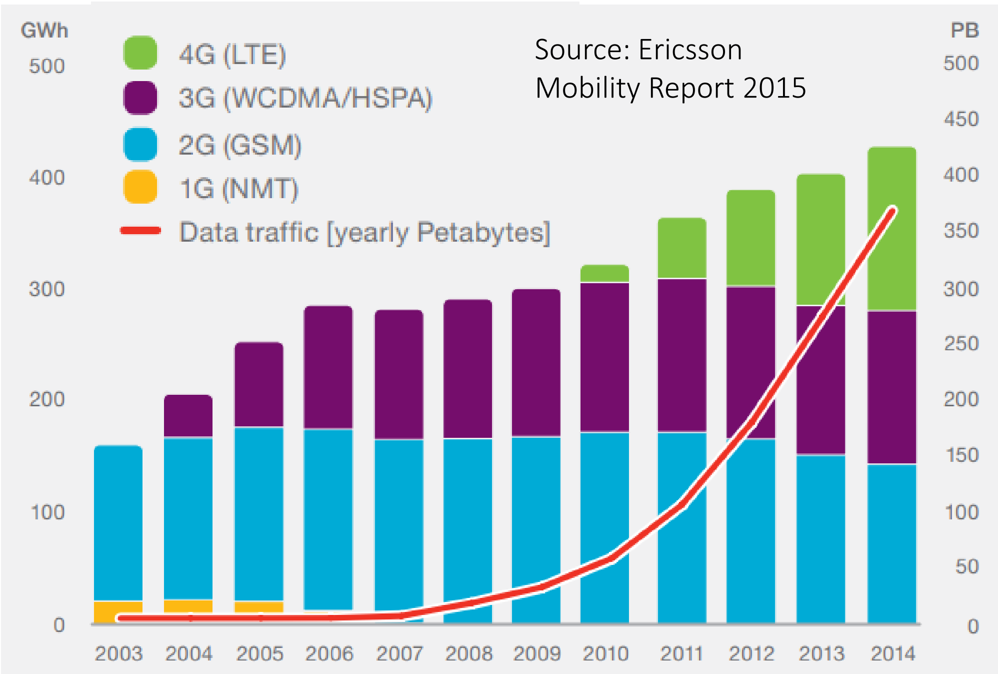
Evolution of the carbon footprint (mobile Internet networks)

Use-phase electricity consumption for access, core and transport networks in Sweden



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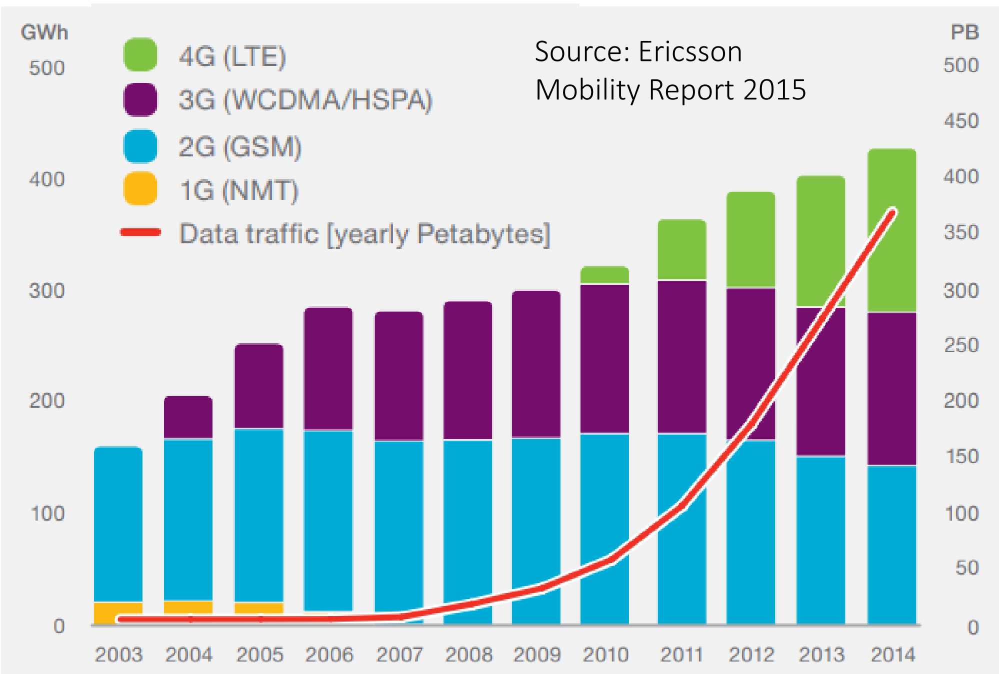
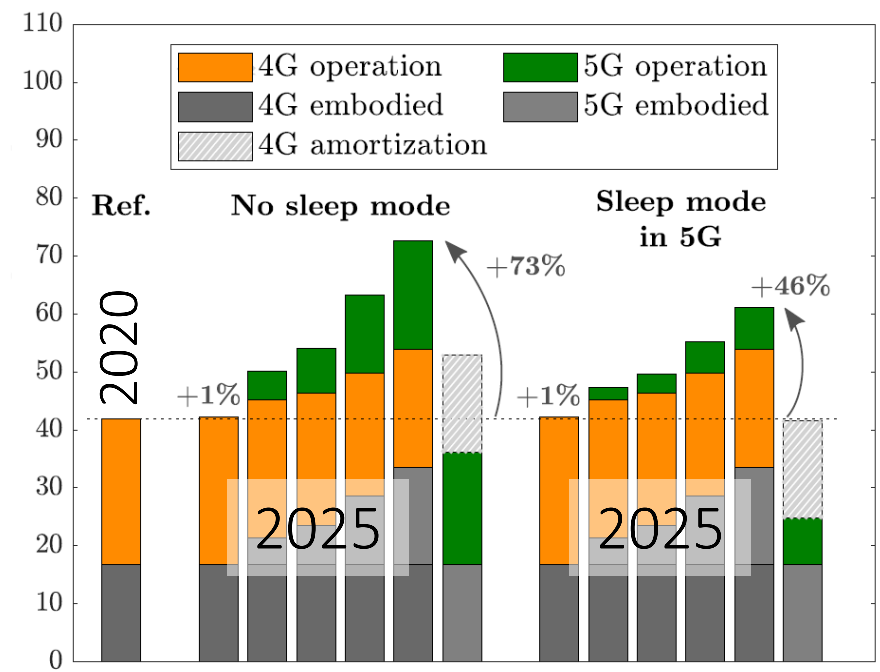


GHG emissions in Belgium for RAN [$ktCO_2e$/year] (assuming 5G sleep mode)



[Golard, Bol and Louveaux, "Evaluation and projection of 4G and 5G RAN energy footprints: The case of Belgium for 2020–2025", ANTES, 2023]

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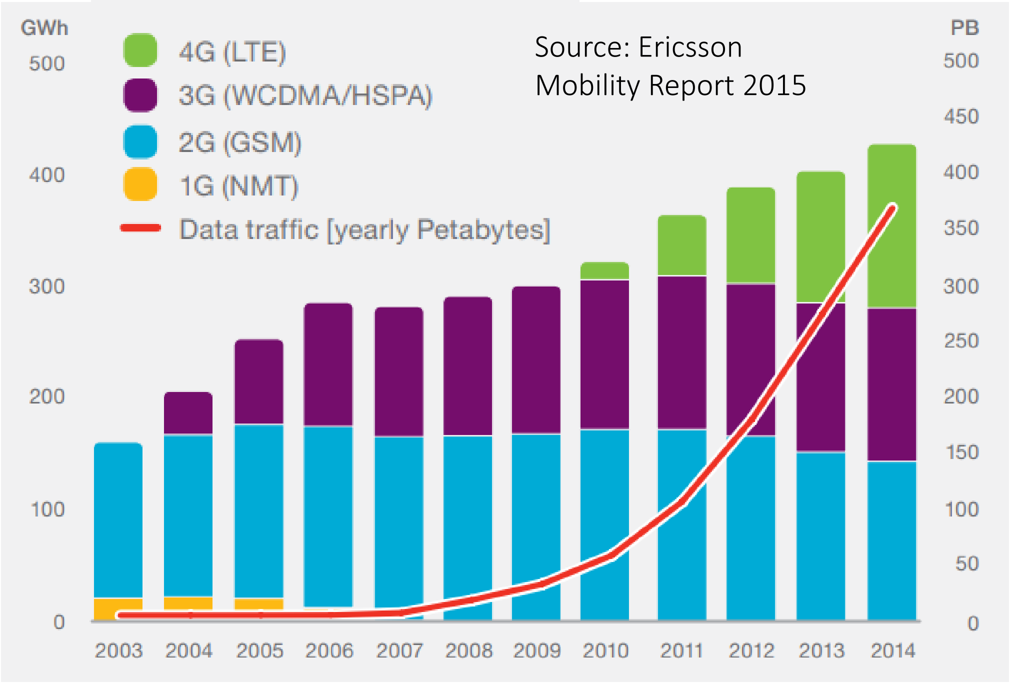

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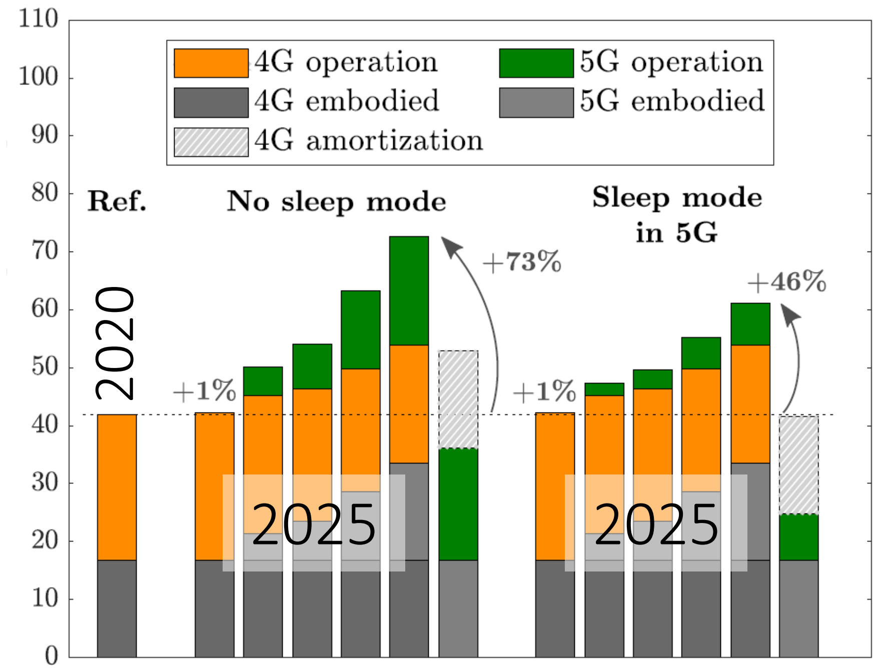

[Golard, Bol and Louveaux, "Evaluation and projection of 4G and 5G RAN energy footprints: The case of Belgium for 2020–2025", ANTES, 2023]

- 4G/5G improved energy efficiency (GB/kWh)
- … but in absence of regulation (traffic limitation decommissioning), deployment of new technologies increase the network carbon footprint

Empirical efficiency-improvement laws

Law	KPI metric	Physical resource	Efficiency CAGR
Moore	Transistors	Silicon wafer	+41%
Cooper	Datarate	RF spectrum	+32%
Koomey	Computations	Electrical energy	+59%

Empirical efficiency-improvement laws

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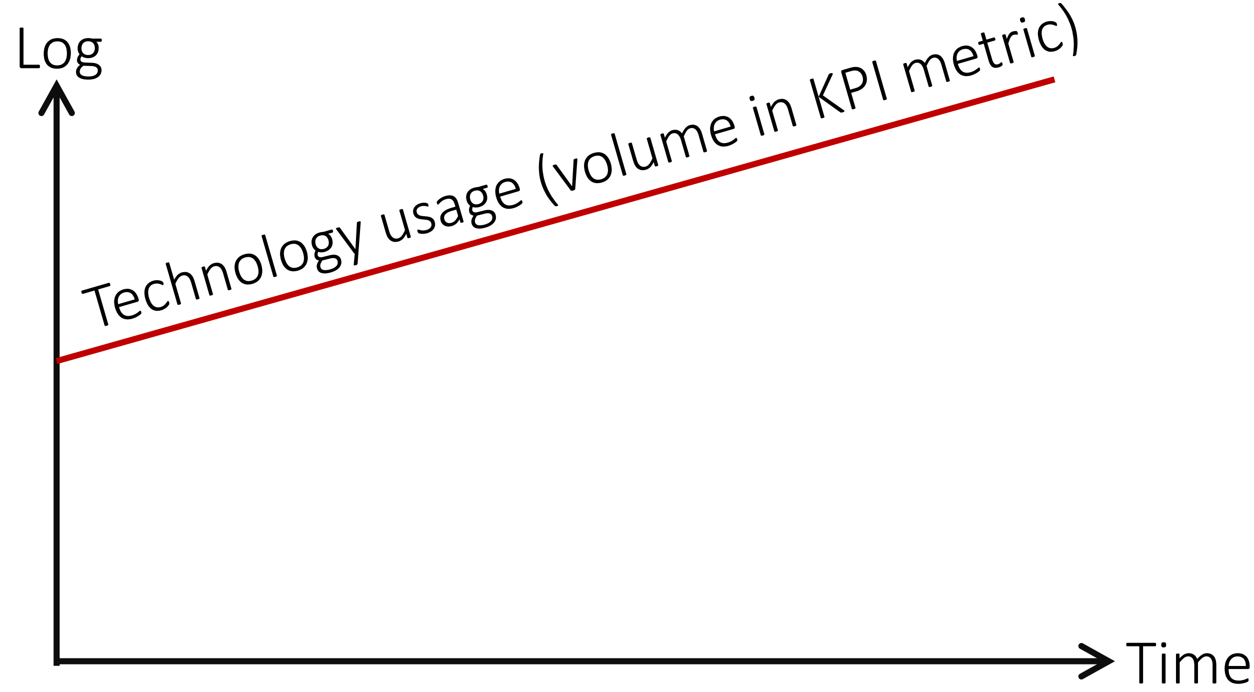

Empirical efficiency-improvement laws

Law	KPI metric	Physical resource	Efficiency CAGR	Intensity CAGR
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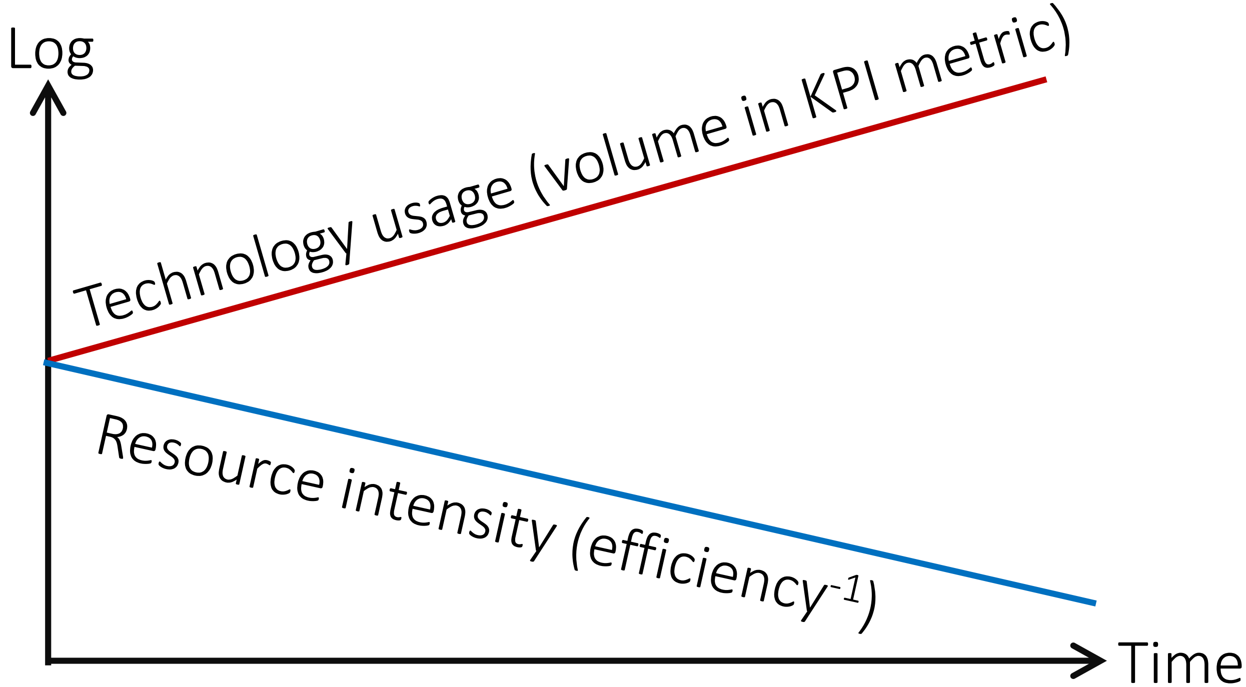

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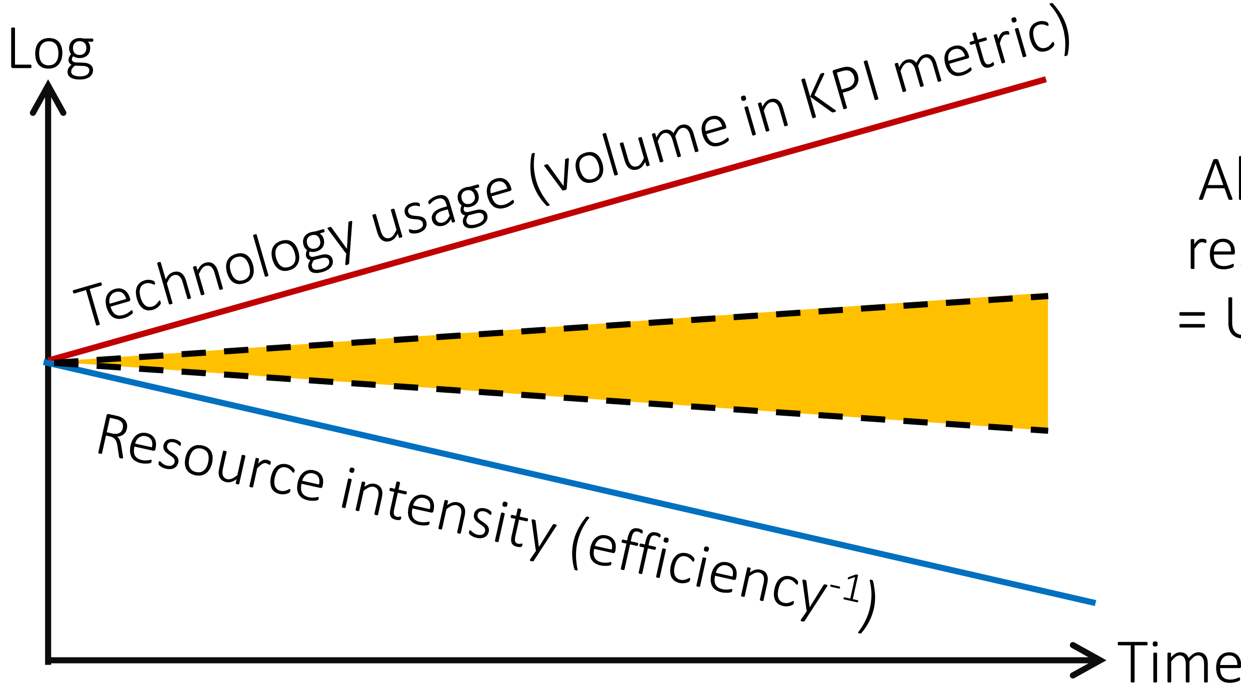

Absolute physical resource footprint = Usage × Intensity

Empirical efficiency-improvement laws

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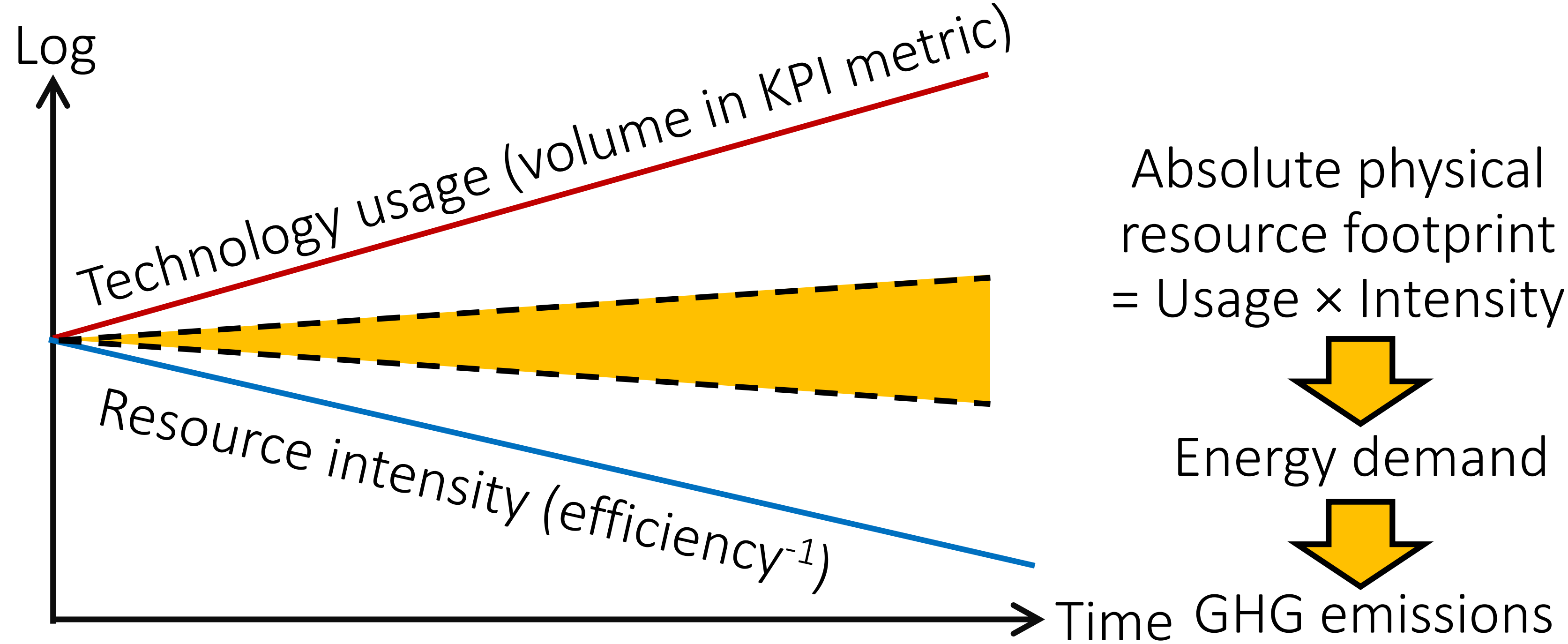


Moore's Law and ICT Innovation in the Anthropocene

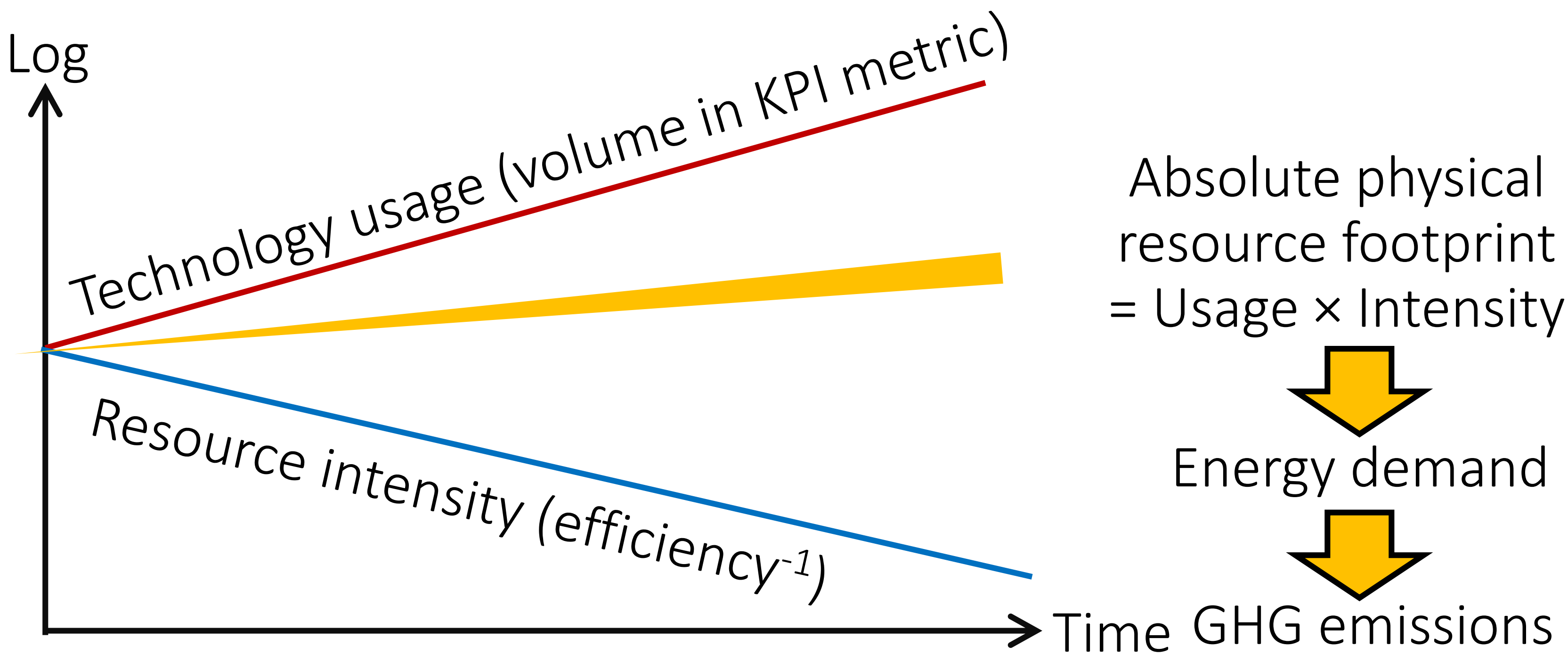
David Bol, Thibault Pirson and Rémi Dekimpe
Electronic Circuits and Systems group, ICTEAM Institute
Université catholique de Louvain, Louvain-la-Neuve, Belgium
david.bol@uclouvain.be

IEEE DATE conf. 2021

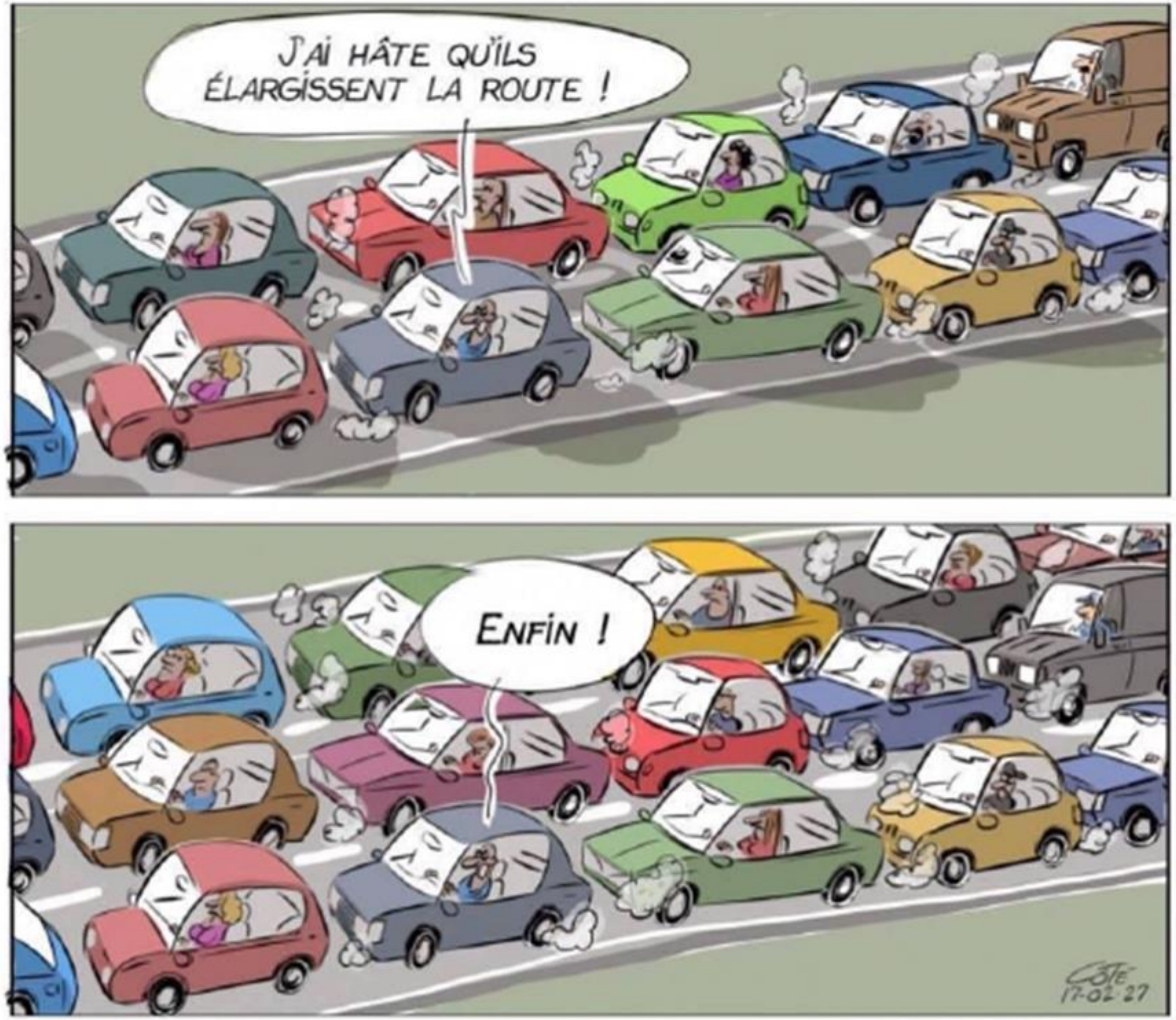
Abstract—In information and communication technologies (ICTs), innovation is intrinsically linked to empirical laws of exponential efficiency improvement such as Moore's law. By following these laws, the industry achieved an amazing relative decoupling between the improvement of key performance indicators (KPIs), such as the number of transistors, from physical

TABLE I
KEY STUDIES OF THE GLOBAL ICT FOOTPRINT.

Source	Reference year	Annual electricity consumption‡ [final TWh]	Annual GHG emissions [$MTCO_2e$]



Rebound effect (Jevons' Paradox)

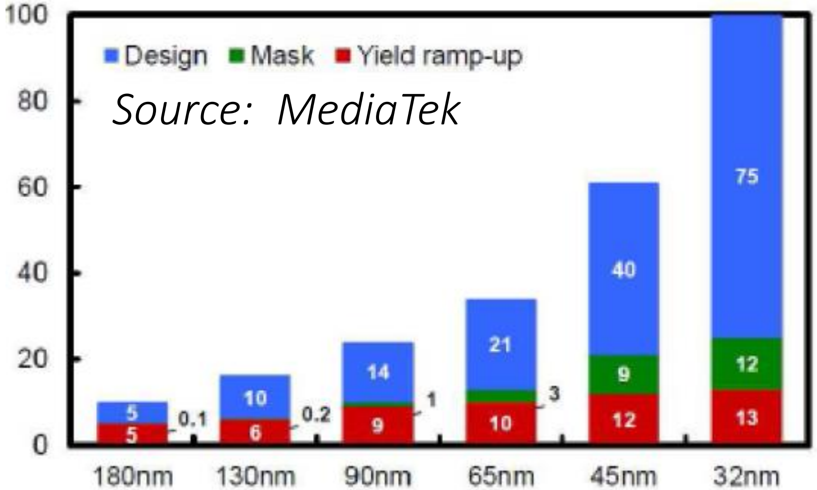


Why does the absolute resource footprint increase in ICT ?

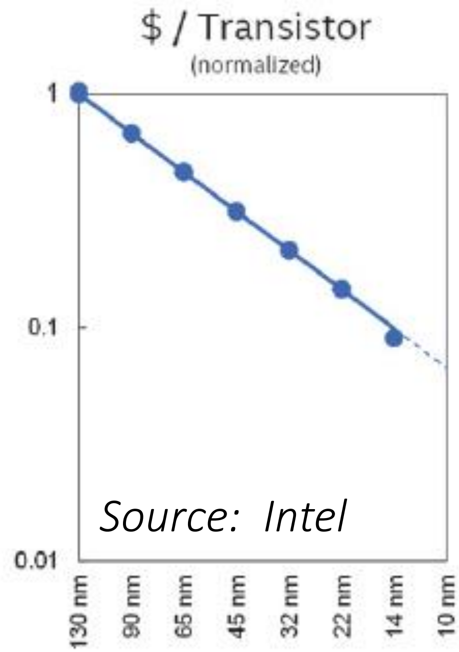
Hypothesis:
Escalating Engineering Costs
(Economics of Technology)

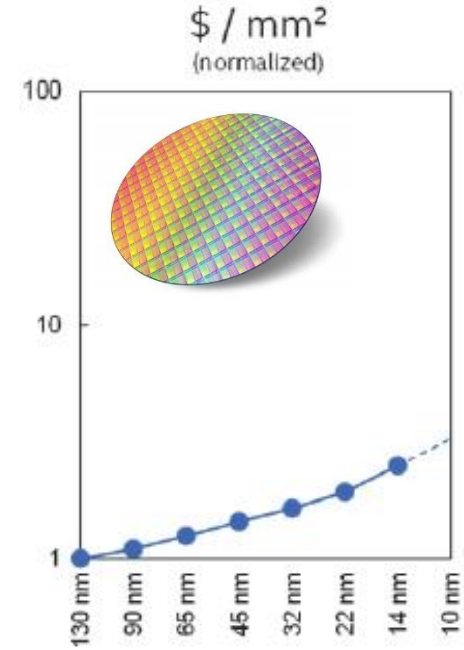
Escalating Engineering Costs

Chip design cost [M$]



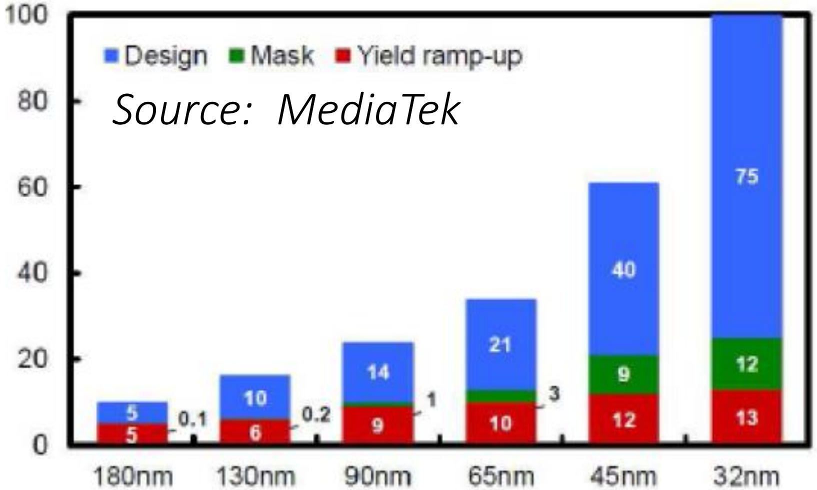
[A. Chang, IEEE Design & Test of Computers, vol. 26, pp. 14-19, 2009]





Escalating Engineering Costs

Chip design cost [M$]



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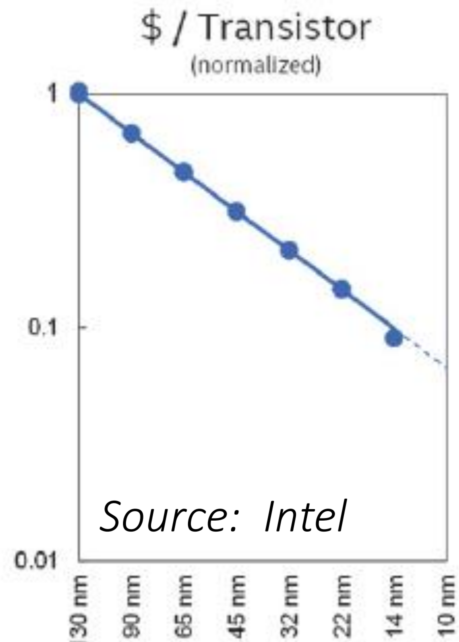
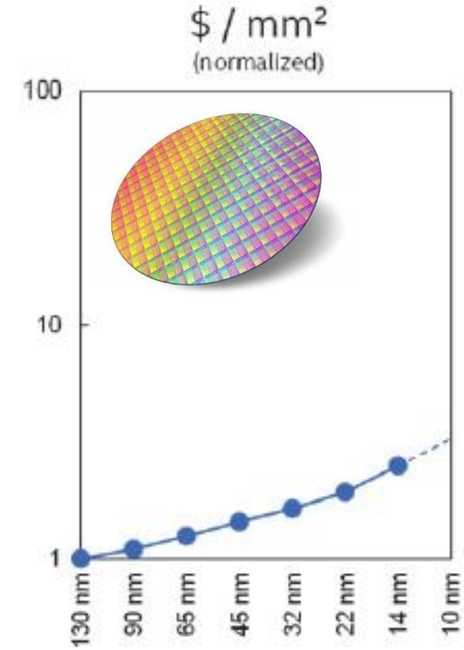
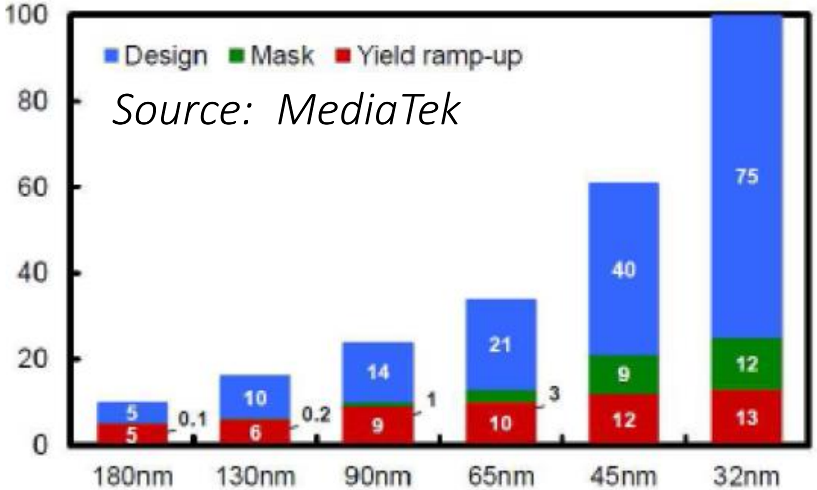




- Fact #1: efficiency KPIs are bounded by a physical limit (e.g. atom size)
- Fact #2: easy improvements have been made first (“low-hanging fruits”)
  → Getting closer to the limit increases complexity & engineering costs

Escalating Engineering Costs

Chip design cost [M$]



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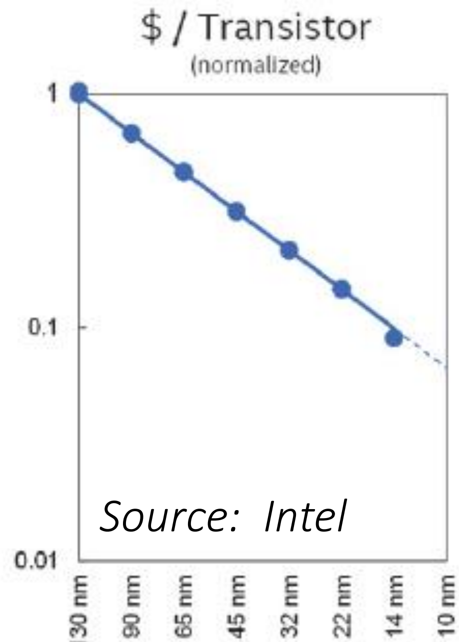
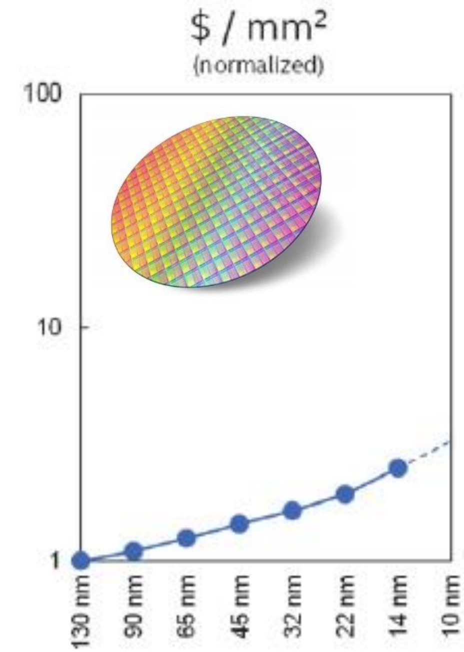




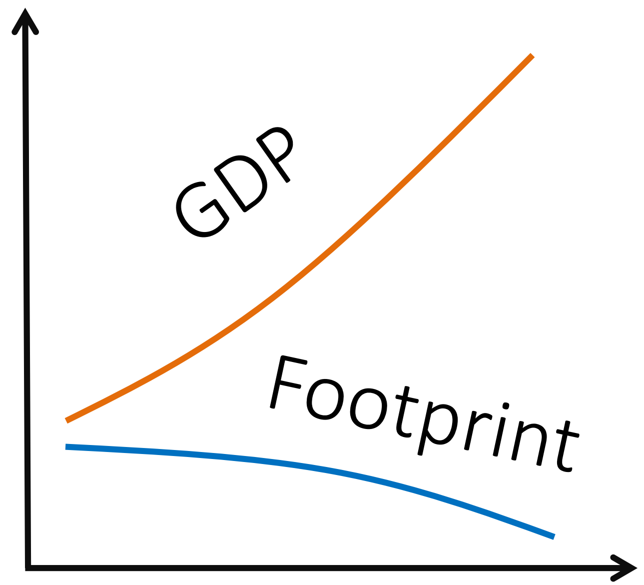
- Fact #1: efficiency KPIs are bounded by a physical limit (e.g. atom size)
- Fact #2: easy improvements have been made first ("low-hanging fruits")
  → Getting closer to the limit increases complexity & engineering costs
- Result: in general in ICT, return on investment (RoI) is generated by increasing the sales and production volumes
  → Increases the usage of the physical resource (wafers)

Can we decouple the tech. usage from the environmental footprint ?

Hypothesis :

The Impossibility of « Green Growth » (Ecological Economics)

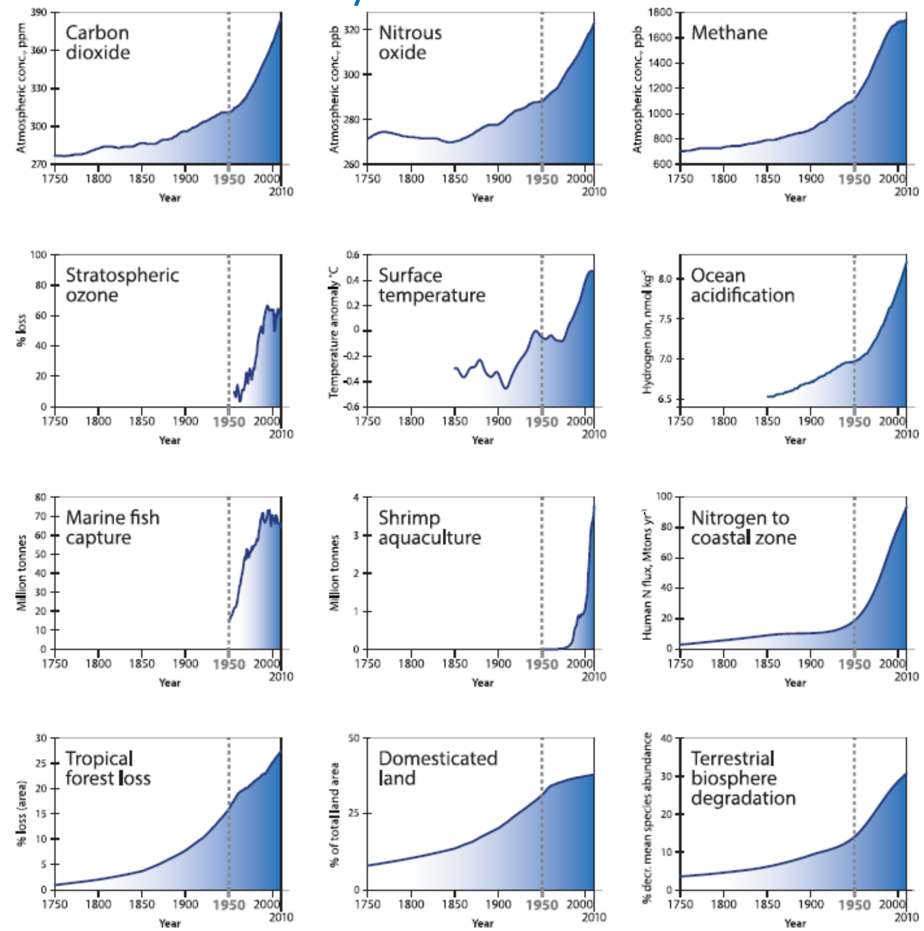
The Impossibility of « Green Growth »



Green growth = the absolute decoupling of the GDP growth from the ecological footprint

A bit of history: the Great Acceleration

Earth-system indicators

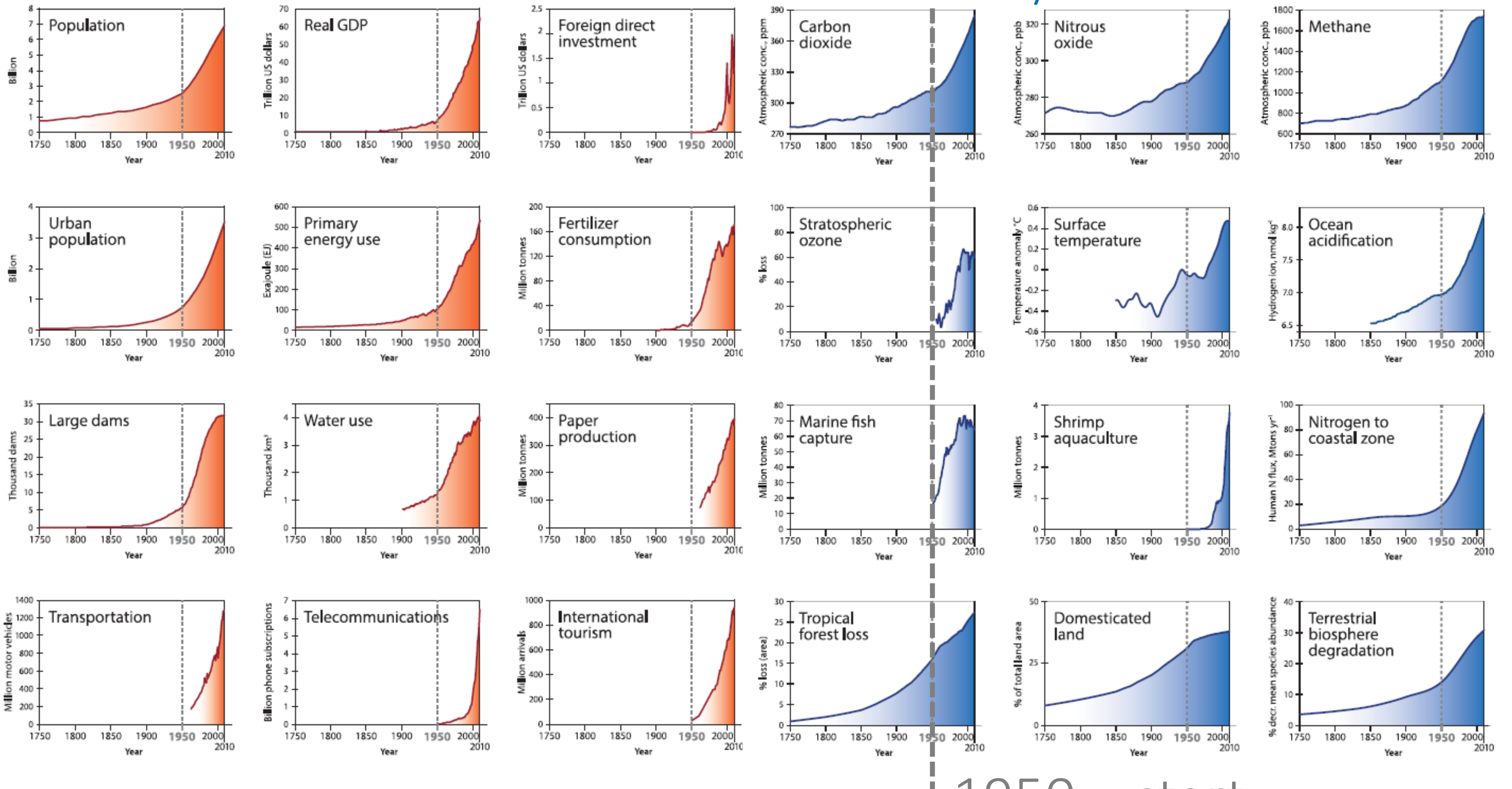


[W. Steffen et al, « The trajectory of the Anthropocene: The Great Acceleration », in Anthropocene Review, 2015]

A bit of history: the Great Acceleration

Socio-economic indicators

Earth-system indicators

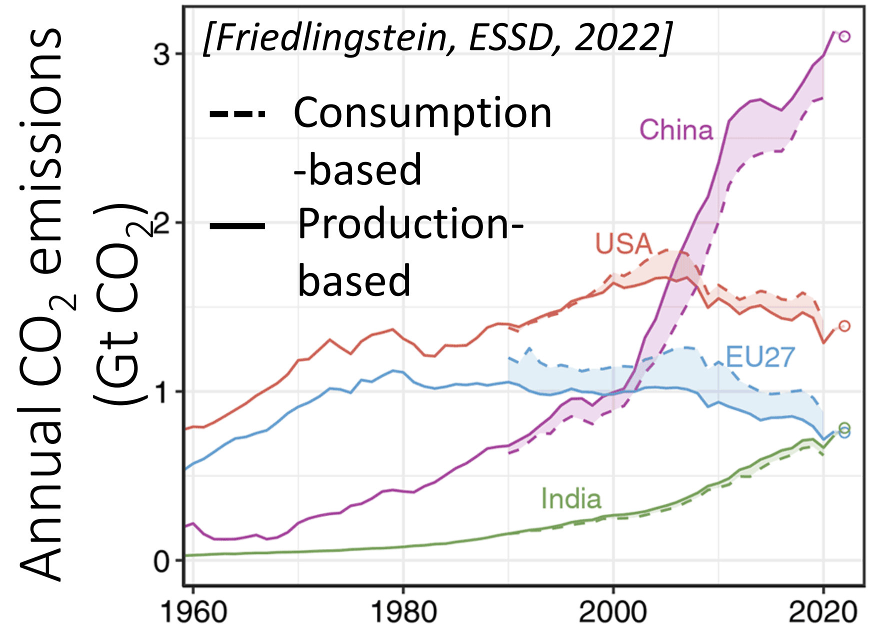


1950 = start of the Anthropocene

[W. Steffen et al, « The trajectory of the Anthropocene: The Great Acceleration », in Anthropocene Review, 2015]

The Impossibility of « Green Growth »

- Can only be studied at the global world scale because of rebound effects and problem & cost shifting issues *[Parrique, "Decoupling Debunked – Evidence and Arguments against Green Growth as a Sole Strategy for Sustainability", 2019]*



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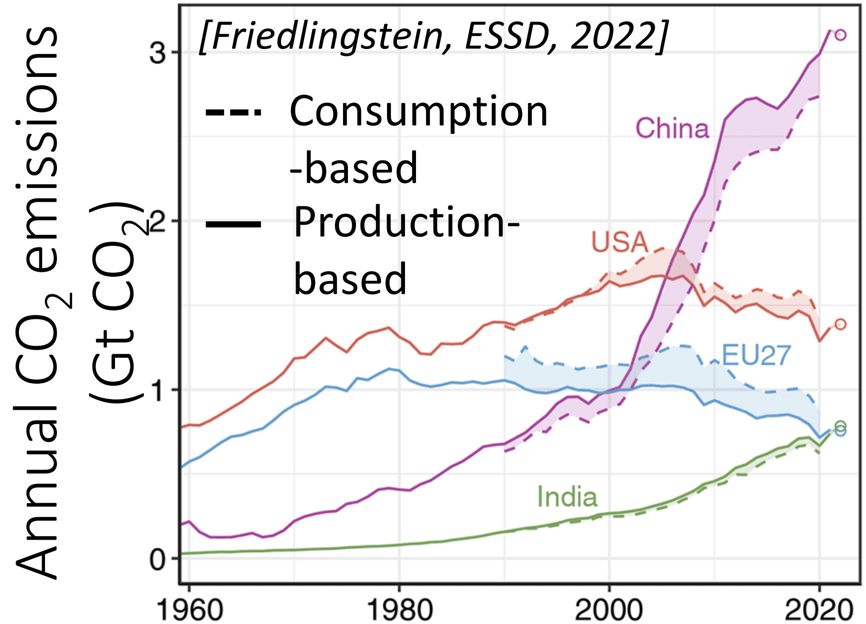
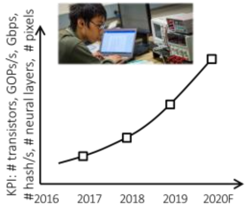


- Absolute decoupling has never been observed so far at large scale *[Jackson, 2009][Parrique, 2019][Hyckel and Kallis, 2020]*
- Betting on reaching the carbon neutrality with green growth solely fueled by a massive energy transition is risky

Faith in technological progress

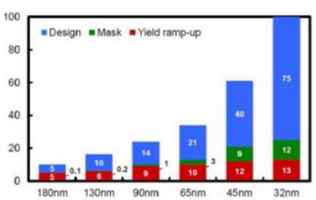
Financial economy

Race
to innovation



Physical limits
on KPI efficiency

Escalating
engineering
costs



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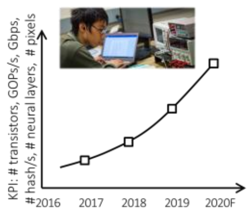
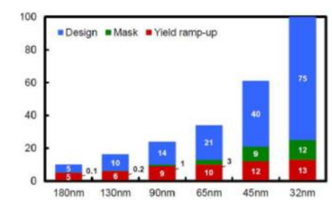


Economic growth target in the real economy

Questionable strategies for increasing tech. usage

Physical limits on KPI efficiency

Escalating engineering costs



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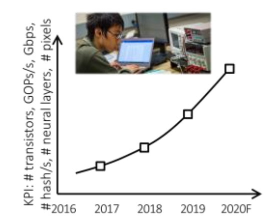
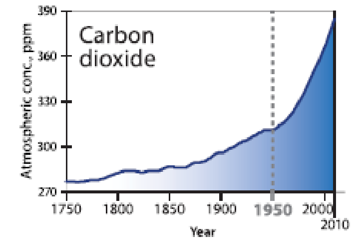


Impossibility
of “green growth”

Increase of the environmental footprint of ICT



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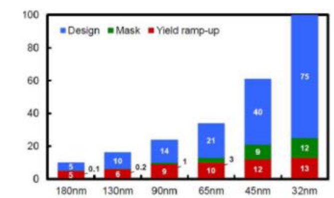

Faith in technological progress

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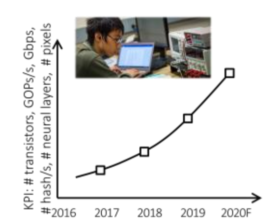
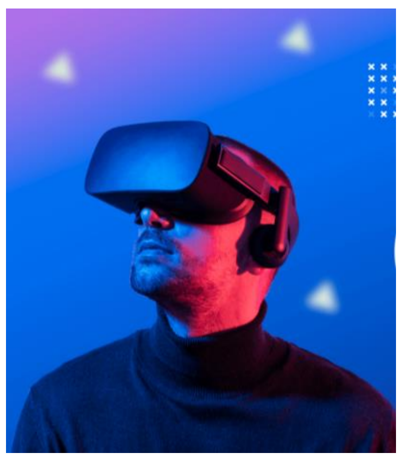
Race
to innovation



Are these worth the cost ?



Citizen protest

Water resources: 800 people demonstrate in front of STMicroelectronics in Isère

4/1/2023, 2:08:54 PM

Source: Teller Report

Outline

- Context: exceeded planetary boundaries
- Should the ICT carbon footprint be reduced?
- Lock-in situation in electronics:
  The pursuit of efficiency causes
  an increase of the ICT energy demand
- Analysis of open-source chip design ecosystem
- How to change course ?

A bit of history again

- 2000 OpenCores.org
- 2010 UC Berkeley RISC-V "OS standard" initiative
- 2013 ETH Zurich PULP research
- 2015 RISC-V foundation
- 2019 ARM Design-Start program
  → ARM academic access program
- 2020 Google and SkyWater collaboration
  on OS ASIC prototyping
- 2021 PICO program from IEEE SSCS

Motivations for OS chip design 1

A. From IC design researchers :
(opinions collected from local researchers):
- Transparency on research results
- Democratization of chip design activity with OS EDA tools and PDKs
- Easier system-level design based on OS IP blocks

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(deduced from *[Rabaey, "Restoring the magic in design", IEEE, DATE 2023]*)

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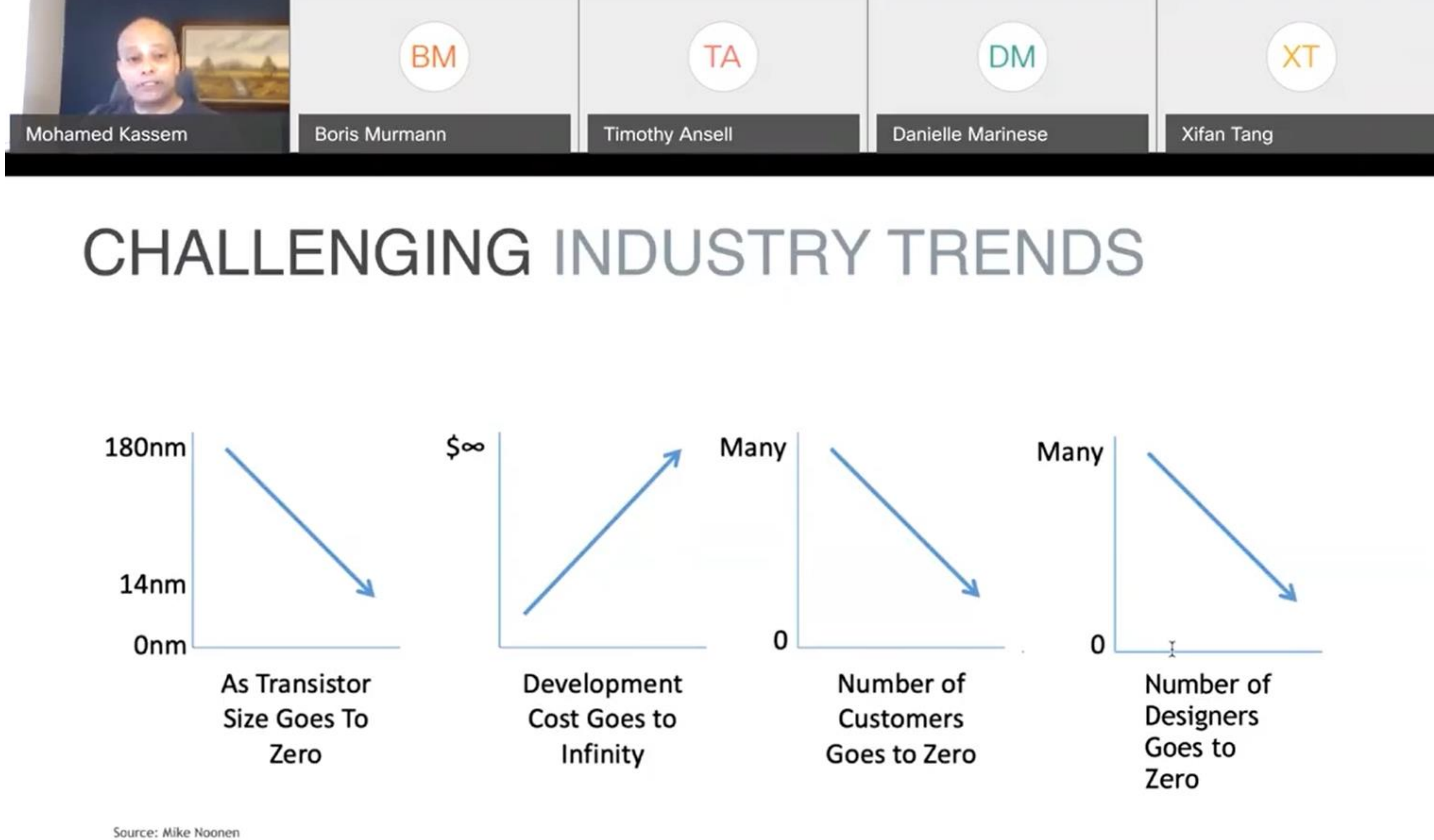
C. From public institutions
(deduced from *["The impact of Open Source ...", report for the EC, 2021]*)

- Independency from foreign major EDA and IP vendors
- Creation of start-ups



« This is actually how the industry is going and it needs to be reversed »

Source: M. Kassem, « 45 Chips in 30 Days: Open Source ASIC at its best! », IEEE SSCD workshop Democratizing IC Design, 2021

Motivations for OS chip design 2

D. From IP providers & EDA tool providers : (hypothesis)
   - Outsource R&D at low cost

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- Reduce access cost to IP blocks and EDA tools (?)

Motivations for OS chip design 2

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E. From fabless chip design companies : (hypothesis)

- Increase the numbers of engineers to hire by attracting more students in chip design
- Reduce access cost to IP blocks and EDA tools (?)

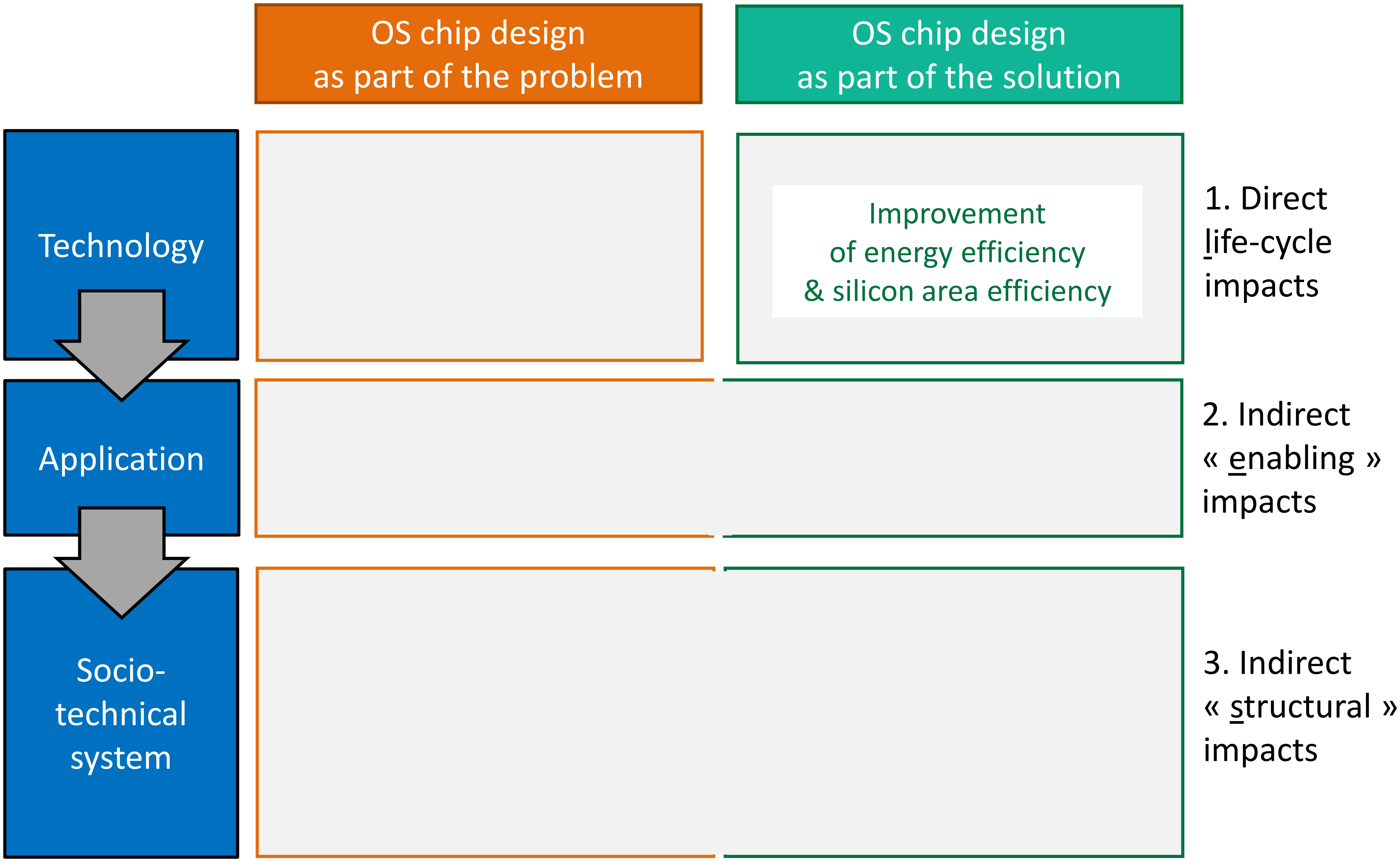
F. From semiconductor foundries : (hypothesis)

- Increase the demand for chip production from new chip products and from larger chips (more IP blocks)

Prospective environmental impacts

	OS chip design as part of the problem	OS chip design as part of the solution	
Technology			1. Direct life-cycle impacts
Application			2. Indirect « enabling » impacts
Socio-technical system			3. Indirect « structural » impacts

Prospective environmental impacts



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Prospective environmental impacts

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Technology	Increase of absolute silicon area & power consumption	Improvement of energy efficiency & silicon area efficiency	1. Direct life-cycle impacts
Application	More applications enabled		2. Indirect « enabling » impacts
Socio-technical system	Increased chip production and deployment volumes Public investment not available for other sectors Labor and human creativity not available for other sectors		3. Indirect « structural » impacts

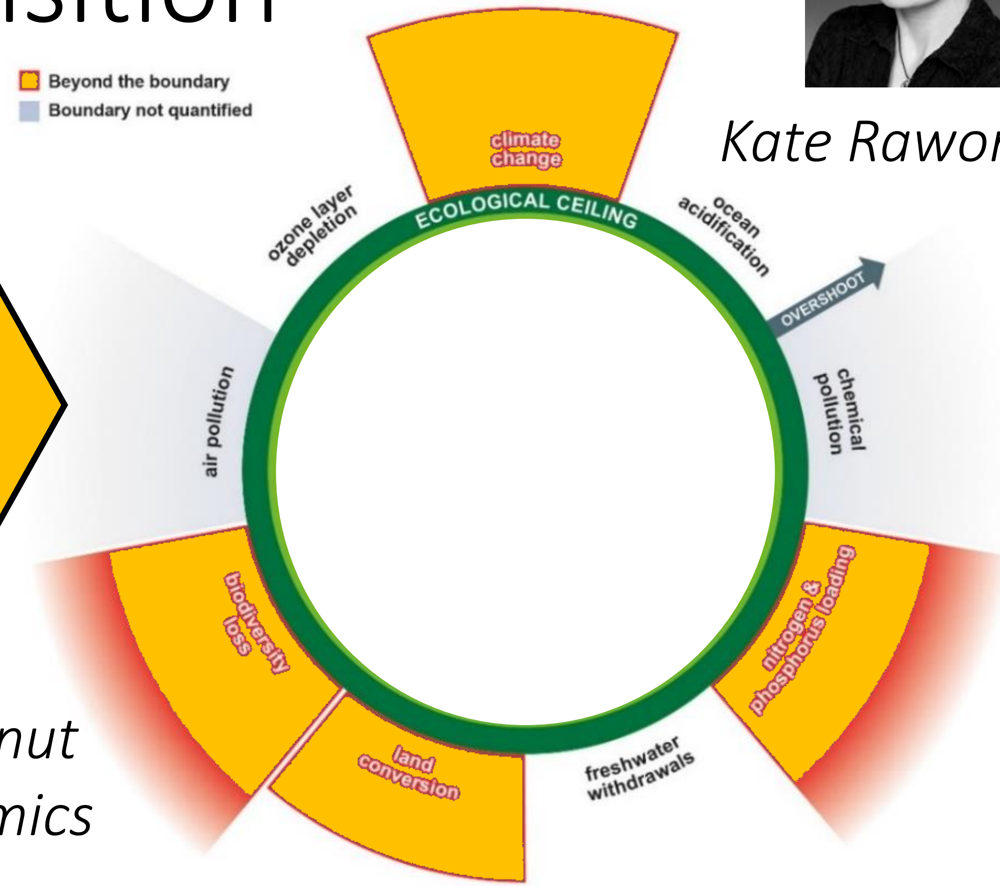
How could we change course ?

Socio-ecological transition

Socio-ecological transition

Kate Raworth

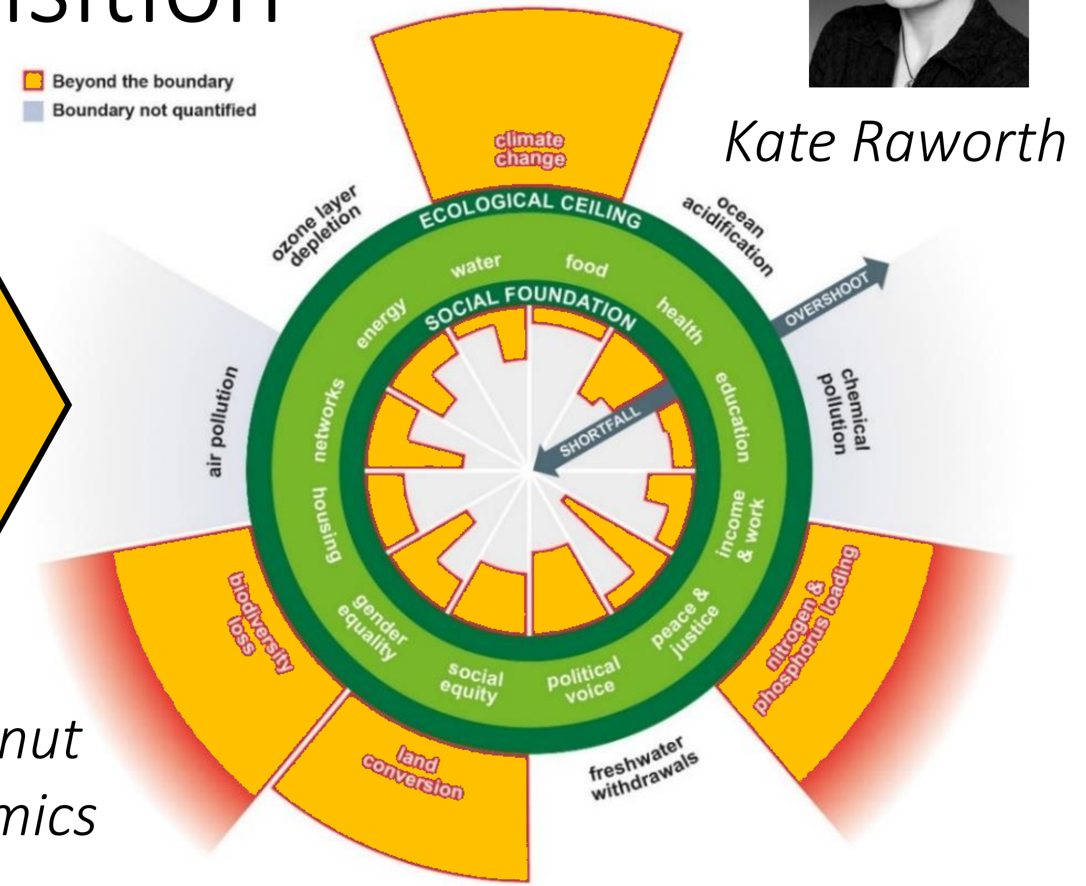
Socio-ecological transition



Doughnut Economics

Socio-ecological transition

Socio-ecological transition



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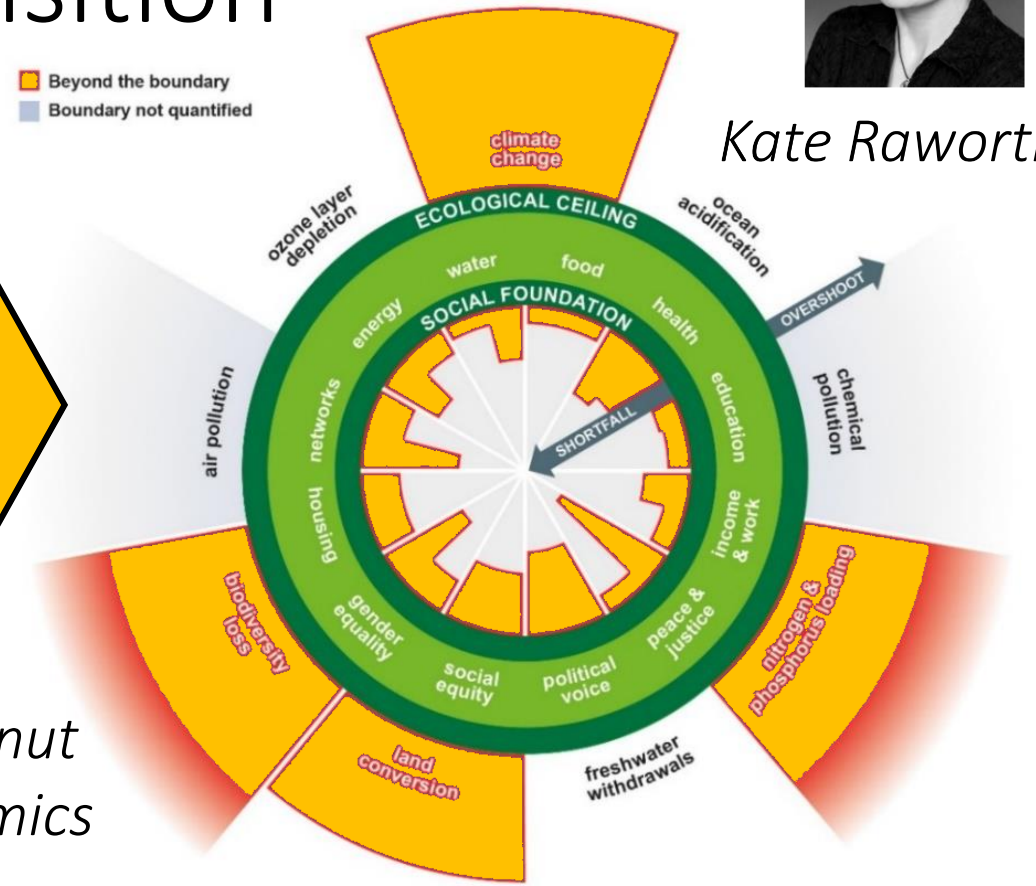
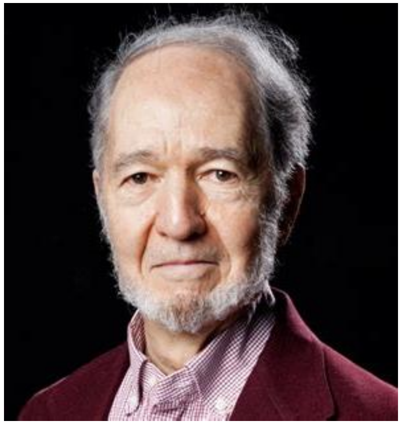


Doughnut Economics

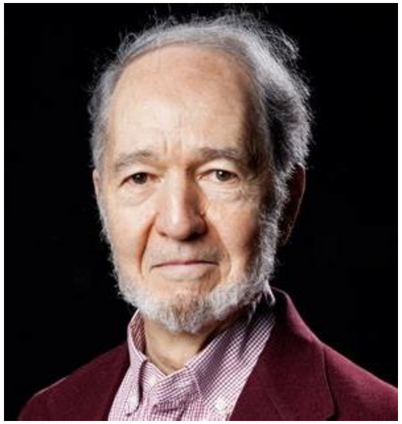
Towards a socio-technical model
which targets human well-being (social floor)
within planet boundaries (ecological ceiling)

Avoiding the collapse



- Collapse definition by Prof. Jared Diamond:
  « a drastic decrease in human population size and/or political/economic/social complexity, over a considerable area, for an extended time. »

Avoiding the collapse



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Failed

- Did not detect/ understand the problem
- Did not act fast/strong enough

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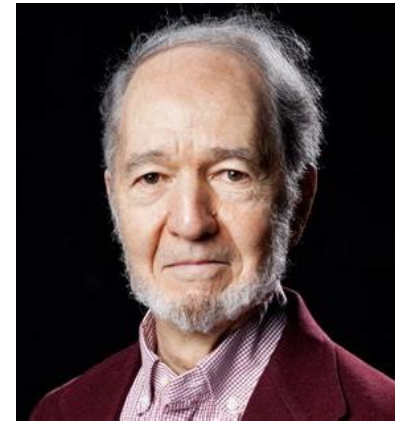
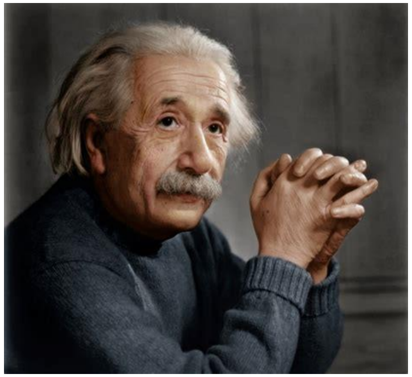


Failed

Succeeded

- Did not detect/ understand the problem
- Did not act fast/strong enough

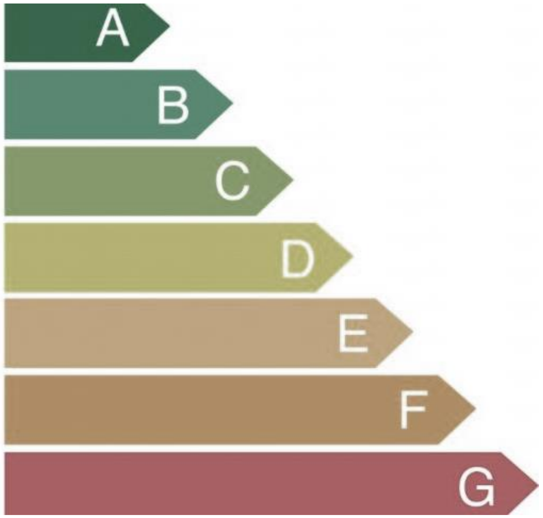
- Adopted a long-term plan
- Revised fundamentally their cultural and ethical values



Albert Einstein

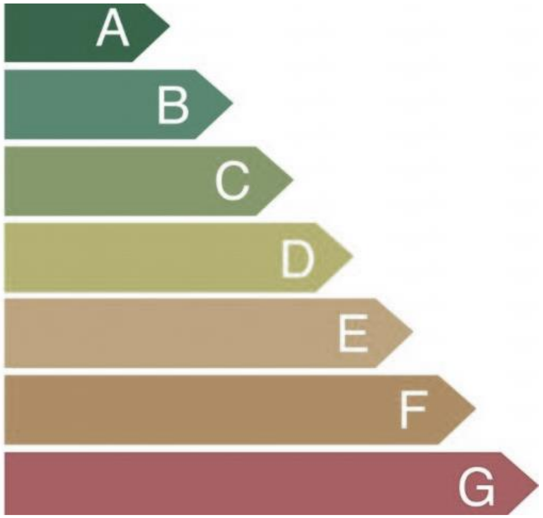
We cannot solve our problems with the same thinking we used when we created them.

Socio-ecological transition in ICT research



Efficiency
(energy and/or resource)

Socio-ecological transition in ICT research

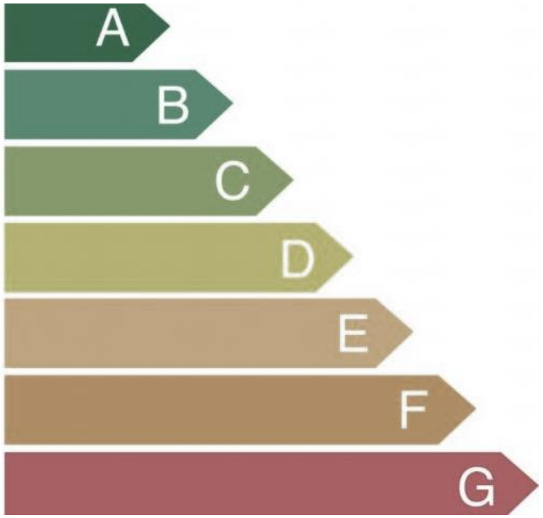


Efficiency
(energy and/or resource)

+

Post-growth sobriety
(strict selection of applications based on <u>clear</u> and <u>demonstrated</u> societal and/or ecological benefits)

Socio-ecological transition in ICT research



Efficiency
(energy and/or resource)

+

Post-growth sobriety
(strict selection of applications based on clear and demonstrated societal and/or ecological benefits)

Quitting the blind faith in technology
(i.e. a dominant ideology called technological utopianism)

Concluding open question:

How could Humanity
agree on meaningful applications
in a fair, democratic and informed
(based on science) way ?

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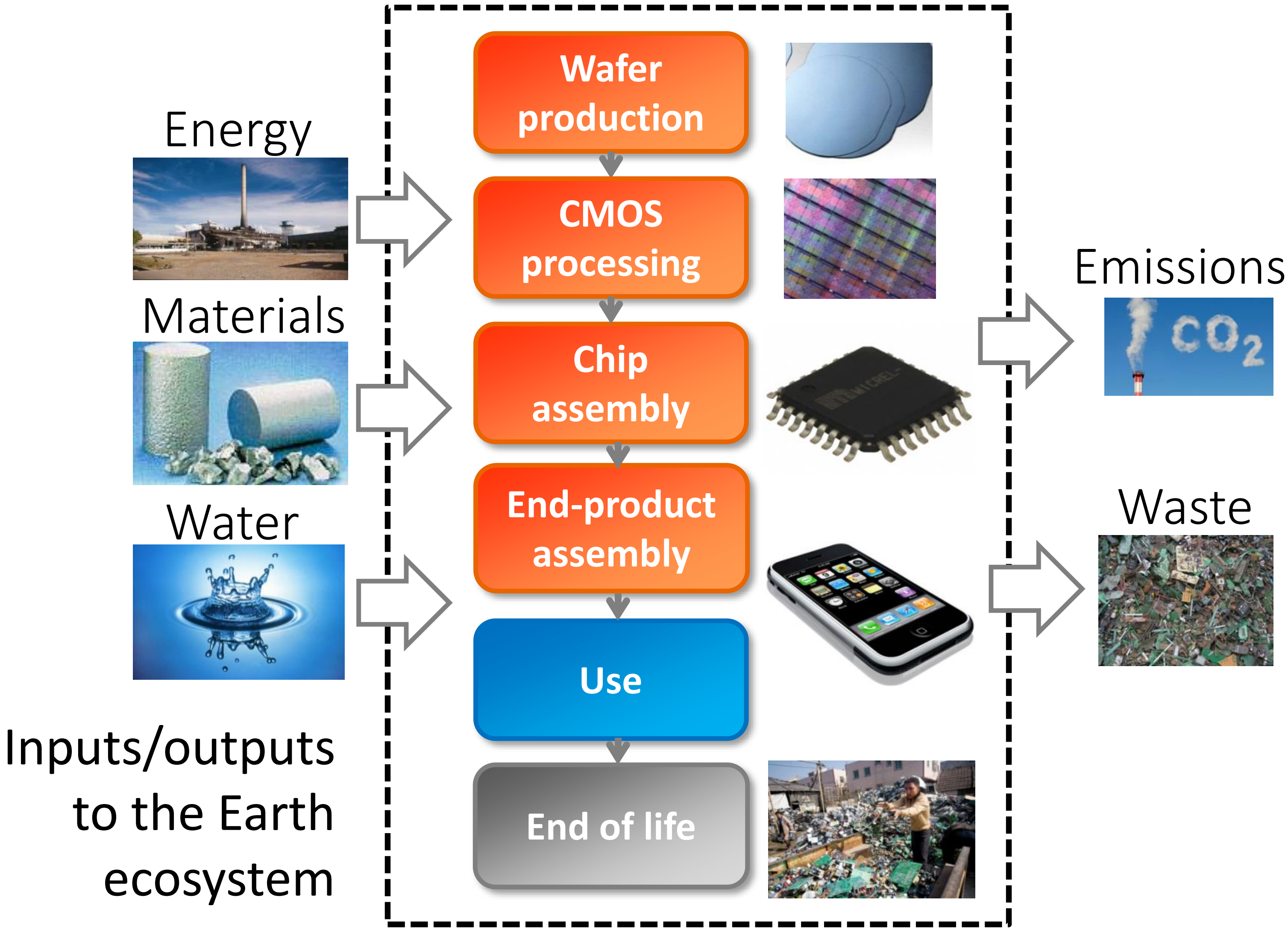
Thank you!

(waiting for the discussion)

This work was supported by the Walloon Region and EU region under FEDER project IDEES and the F.R.S.-FNRS of Belgium.

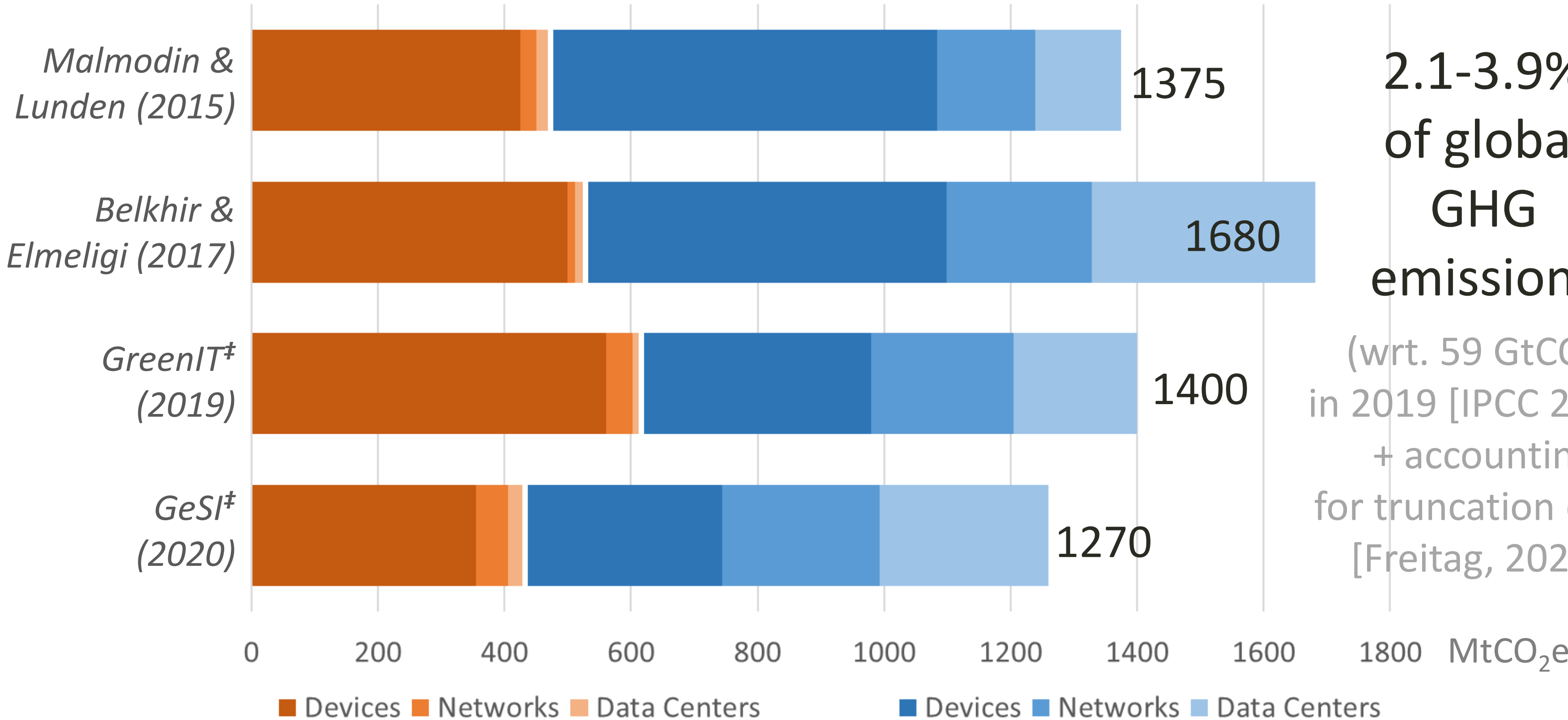
Backup slides

Life "cycle" of electronic products



[D. Bol, S. Boyd and D. Dornfeld, « Application-aware LCA of semiconductors: life-cycle energy of microprocessors from high-performance 32nm CPU to ultra-low-power 130nm MCU », in Proc. IEEE ISSST, 2011]

The carbon footprint of the ICT sector



2.1-3.9% of global GHG emissions

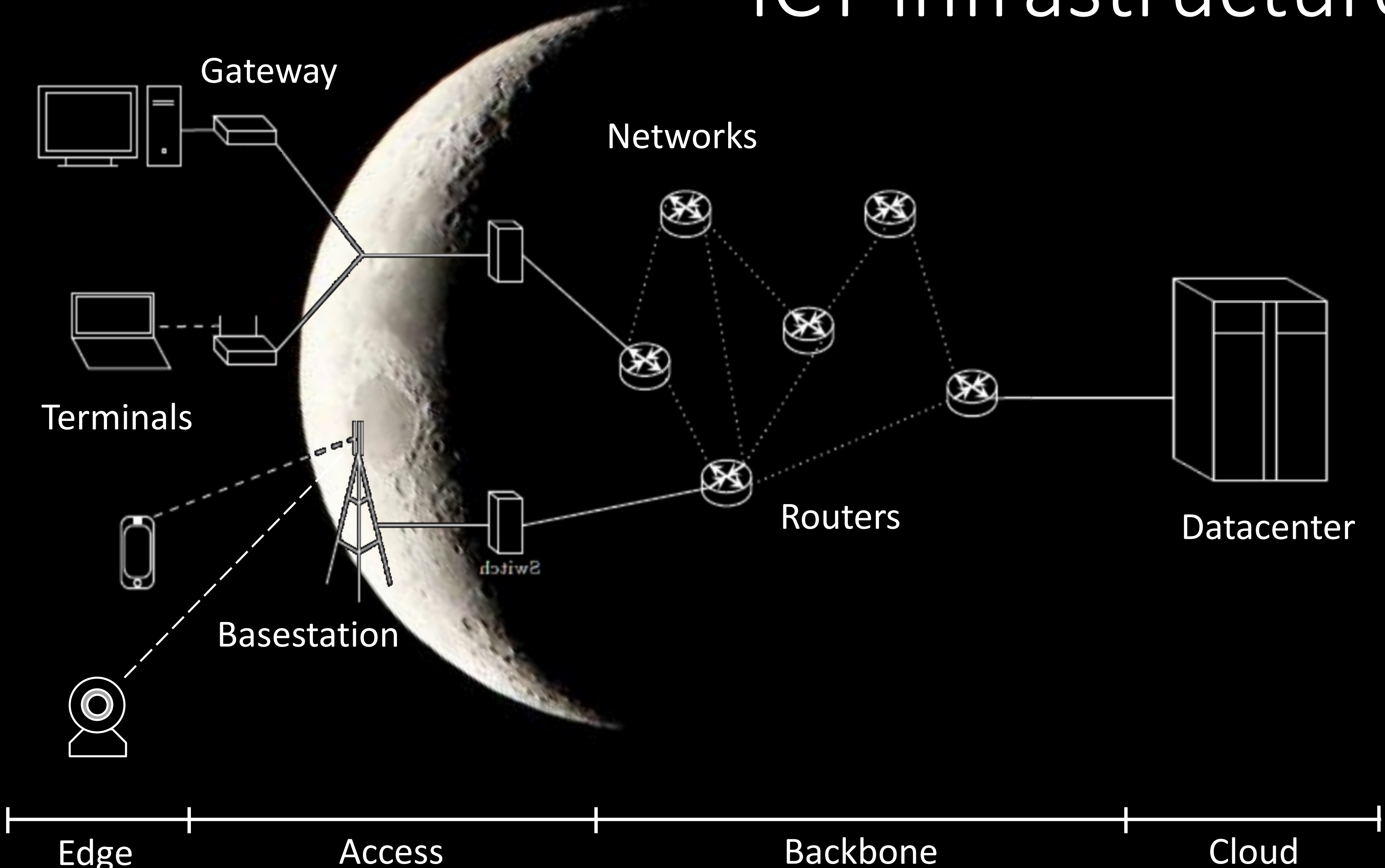
(wrt. 59 $GtCO_2e$ in 2019 [IPCC 2022], + accounting for truncation error [Freitag, 2021])

Production — Use (6-7% of global electricity)

Devices includes TVs and printers, ‡sources not peer-reviewed

Sources: Malmodin & Lunden, "The Energy and Carbon Footprint of the Global ICT and E&M Sectors 2010–2015", Sustainability, 2018 ; Belkhir & Elmeligi, "Assessing ICT global emissions footprint: trends to 2040 & recommendations", Jour. Clean. Prod., 2018 ; F. Bordage, GreenIT.fr, "Environmental footprint of the digital world", 2019 ; GeSI, "SMARTer 2020: The Role of ICT in Driving a Sustainable Future", 2012.

Digital services run on the physical ICT infrastructure

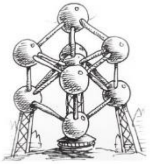


It's not only about climate and energy

Coltan mine in North Kivu (Congo)
Copyright: Stefano Stranges

E-waste informal recycling area in Guiyu (China)

E-waste generated in 2018: 4M tons = 400 ×  (weight)

1500 ×  (weight)

Why do technology engineers aim to improve performance ?

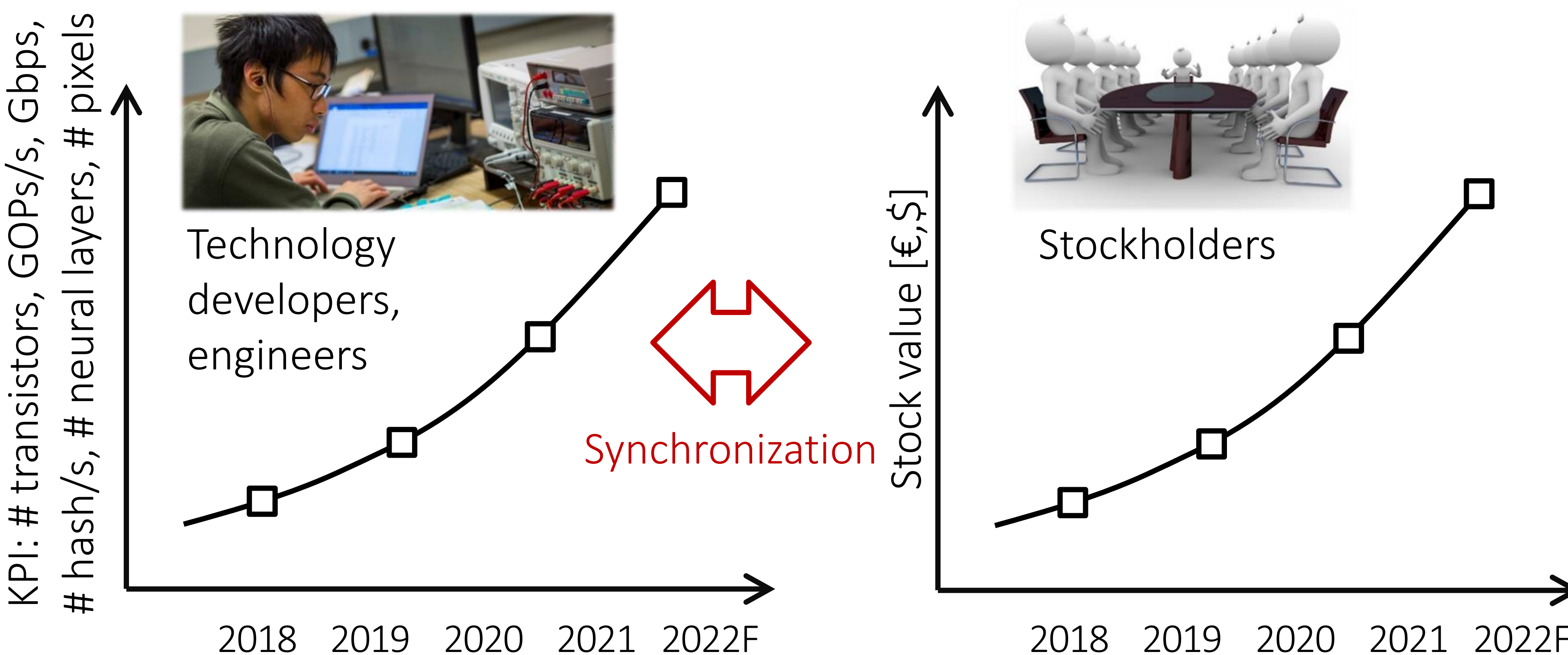
Thesis #1 :
The Race to Innovation
(Sociology/Anthropology of Technology)

Thesis #1: the Race to Innovation

- Fact: the "Great Inventions of the 20th century" *[Gordon, 2018]* improved the living standards
- Result: humanity has a <u>deep faith in the social benefits of technological progress</u> *[Potts, 2018]*
- Fact: since 1980, huge capitalization available on the stock market lead to the <u>*financial economy*</u>
- Result: companies compete to attract capitals by promising stock value growth (< speculation) *[Krier, 2009][Mundt, 2014][Davis, 2018][Gomez, 2019]*

The Race to Innovation is one of the few means for companies to attract capitals [Dallyn, 2011][Gomez, 2019]

Performance-driven innovation in the financial economy



20 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 48, NO. 1, JANUARY 2013

SleepWalker: A 25-MHz 0.4-V Sub-mm^2 7-μW/MHz Microcontroller in 65-nm LP/GP CMOS for Low-Carbon Wireless Sensor Nodes

David Bol, *Member, IEEE*, Julien De Vos, *Student Member, IEEE*, Cédric Hocquet, François Botman, *Student Member, IEEE*, François Durvaux, Sarah Boyd, Denis Flandre, *Senior Member, IEEE*, and Jean-Didier Legat, *Member, IEEE*

Key performance indicators (KPIs)

***Abstract*—Integrated circuits for wireless sensor nodes (WSNs) targeting the Internet-of-Things (IoT) paradigm require ultralow-power consumption for energy-harvesting operation and low die area for low-cost nodes. As the IoT calls for the deploy-**

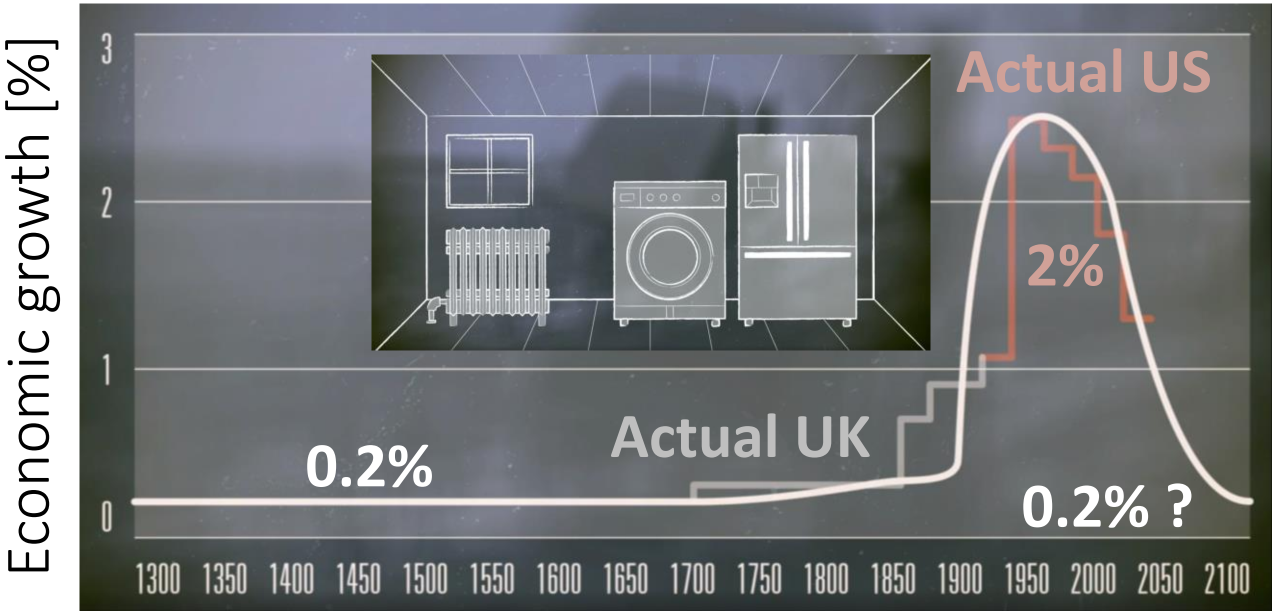
ject [1]. Such WSNs will feature sensing and computing capabilities with memories, energy management and wireless communication to allow interaction with the cloud. The IoT will en-

	Bol, JSSC, 2013	Myers, VLSIC, 2017	Prabhat, ISSCC, 2020	Lee, JSSC, 2020	Paul, JSSC, 2017	Ambiq, ApolloBlue3, 2019	Salvador, ESSCIRC, 2018	Abouzeid, ESSCIRC, 2015	Uytterhoeven, ESSCIRC, 2018	Lallement, JSSC, 2018	Lallement, SSCL, 2019	Höppner, ESSDERC, 2019	This work
CMOS technology	65nm LP/GP	65nm LP	65nm LP	55nm DDC	14nm FinFET	40nm ULP eFlash	90nm ULL eFlash	28nm FDSOI	28nm FDSOI	28nm FDSOI	22nm FDSOI	22nm FDSOI	28nm FDSOI
CPU	oMSP430	CM0+	CM33 SIMD	CM0	x86 IA	CM4F	CM3	CM4F	Zscale	CM0+	CM0+	CM4F	CM0DS
Memory	18kB SRAM	16kB SRAM	128kB ROM + 20kB RAM	8kB SRAM	16kB ROM + 80kB SRAM	384kB SRAM + 1MB Flash	32kB SRAM + 256kB Flash	16kB SRAM	64kB SRAM	8kB SRAM	12kB SRAM	84kB SRAM	64kB SRAM
Closed-loop PVT compensation	UFVR (AVS)	AFS	UFVR (AVS)	AVS+ABB with MEP tracking	×	N/A	UFVR (AVS)	×	×	×	Limited ABB	ABB	UFBR (ABB)
Embedded PM	✓	✓	✓	✓	×	✓	✓	×	×	×	×	×	✓
Max. frequency at MEP supply [MHz]	32	0.2	0.8	5	3.5	96	16	45	66	16	20	180	80
Active power at MEP [µW/MHz]	6.1 @25 MHz	7.6 @0.2 MHz	20 @4 MHz	6.4 @0.5 MHz	27* @3.5 MHz	32.8† @48 MHz	23 @5 MHz	8.9 @45 MHz	8.8 @22 MHz	2.7 @16 MHz	1.13 @20 MHz	6.9 @180 MHz	3.3 @40 MHz
Peak efficiency [DMIPS/mW]	~ 66* (10 DMIPS)	180 (0.24 DMIPS)	95 (7.6 DMIPS)	× (not enough RAM)	~ 74* (7 DMIPS)	58† (93 DMIPS)	82 (9 DMIPS)	215 (86 DMIPS)	126 (24 DMIPS)	× (not enough RAM)	841 (19 DMIPS)	278 (344 DMIPS)	385 (51 DMIPS)
Logic state retention in deep sleep mode	×	✓	×	N/A	✓	✓	✓	N/A	N/A	×	✓	✓	✓
Deep-sleep retention power [nW/kB]	95‡ (18kB RAM)	16 (4kB RAM)	2.5‡ (4kB RAM)	-	79 (80 kB RAM)	220† (8 kB RAM) 17† (384kB RAM)	4.3 (8kB RAM)	-	-	121 (8kB RAM)	308 (12kB RAM)	> 548° (84 kB RAM)	131 (64 kB RAM)
Wake-up time	30 µs	N/A	180 µs	-	> 1 ms	15 µs	N/A	-	-	N/A	N/A	N/A	< 20 µs

How do we increase technology affluence ?

Thesis #3 :
Questionable Growth Strategies (Economics)

Economic Growth Perspectives



Prof. Robert J. Gordon

- Economic growth was enabled by the "Great Inventions of the 20th Century" (combustion engine, water system, electricity)
- To continue the 2% historic GDP growth, future innovations should be as fundamental as the "Great Inventions from the 20th century"

→ KO: the 20th-century growth is a one-off episode in the history of humanity *[Gordon, 2018], ("Secular Stagnation" concept)*

Growth Strategies in ICT

- Strategy A: Addiction mechanisms

Growth Strategies in ICT

Yesterday

Incredible

Today

Outdated

- Strategy A: Addiction mechanisms
- Strategy B: Obsolescence generation

Growth Strategies in ICT

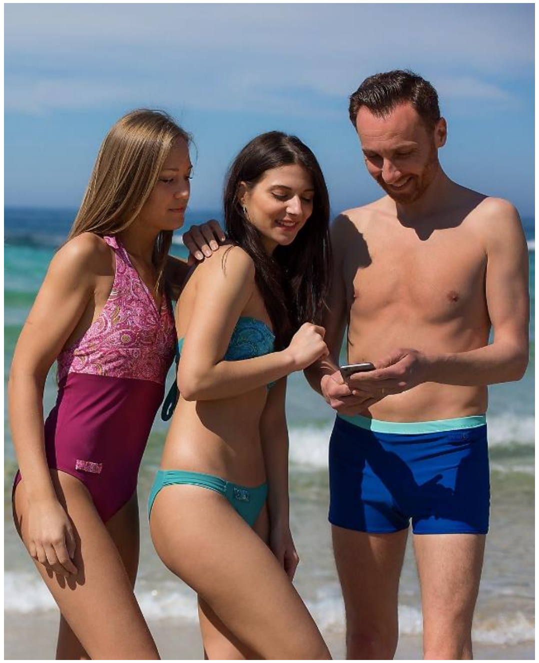
Internet of Shit (IoS) examples

Smart drink bottle

Connected razor

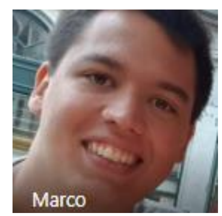
Alexa-enabled shower head

Connected swimwears



- Strategy A: Addiction mechanisms
- Strategy B: Obsolescence generation
- Strategy C: Creation of artificial needs

The socio-ecological transition initiative in the UCLouvain ECS group



Our pillars

(inspired by the Transition Town movement)

Sobriety

Strict selection of a limited set of applicative projects we pursue, chasing potential app. detours

Environment preservation

Systematic footprint analysis of the projects
Direct: LCA of the circuits and systems
Indirect: application

Local organization

Prioritize local field actors + integrate the transition in local university courses

Social link

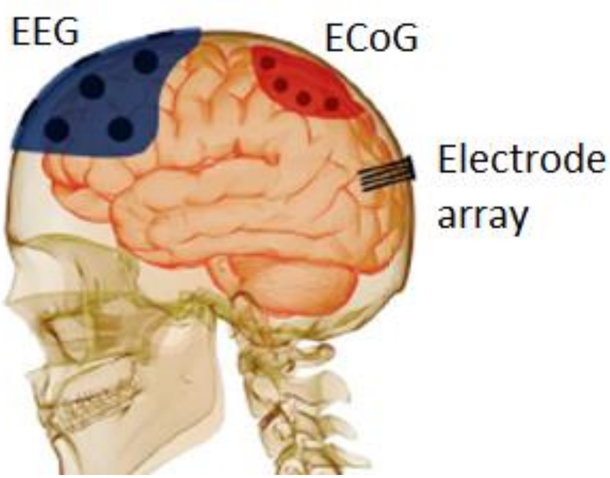
Participative governance + transdisciplinary work (connection with field actors)

Resiliency

Open-source HW/SW ?
Low-tech ?

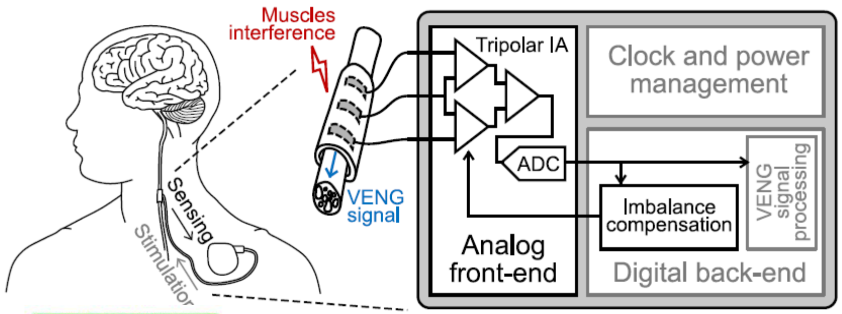
Example A: implanted electronics

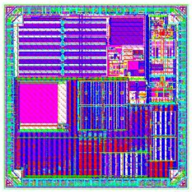
Before: chips for treating epilepsy with closed-loop deep brain stimulation (DBS)



- ✓ Societal benefit (global health)
- ✓ Low absolute ecological footprint
- × High risk of detour (augmented human)

Now: chips for treating epilepsy with closed-loop vagus nerve stimulation (VNS)





[R. Dekimpe and D. Bol, « Mixed-Signal Compensation of Tripolar Cuff Electrode Imbalance in a Low-Noise ENG Analog Front-End », ESSCIRC, 2022]

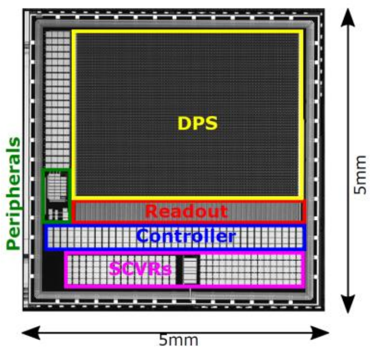
- ✓ Societal benefit (global health)
- ✓ Low absolute ecological footprint
- ✓ Limited risk of detour
- ▪ Technological challenge: very low signal level

ULB

Cliniques universitaires SAINT-LUC

Example B: vision systems

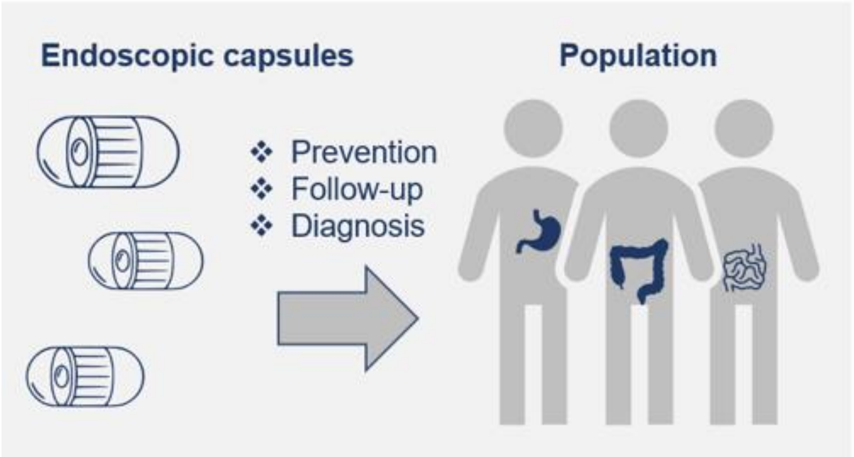
Before: ultra-low-power chips <u>for motion detection and face recognition</u>



[Bol, Symp. VLSI, 2014] [Couniot, JSSC, 2015, [Lefebvre, ISSCC, 2021]

- ✓ Low <u>relative</u> ecological footprint
- × No social benefit (futile applications)
- × High risk of detour (surveillance capitalism)

Now: ultra-low-power system <u>for capsule endoscopy</u>



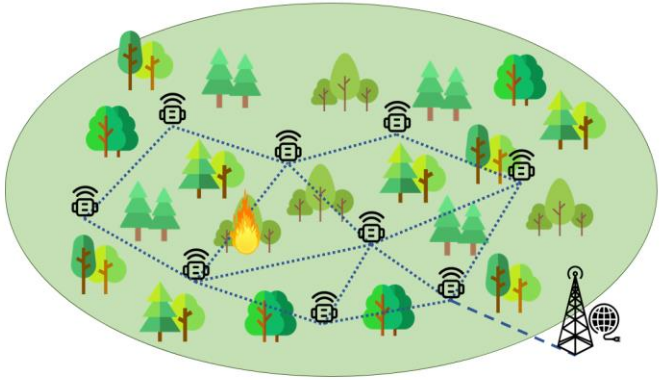
- ✓ Low <u>relative</u> ecological footprint
- ✓ Limited risk of detour
- ▪ Technological challenge: high diagnosis yield at low power
- ▪ Non technological challenge: high acceptance rate by the patients

Example C: IoT sensors

Before: ultra-low-power miniature batteryless solar-powered voice recognition

- ✓ Direct footprint reduction
- × Questionable need
- × High risk of rebound & detour

Now: large-scale detection of abnormal events in natural ecosystems (wildfires, illegal poaching, sawing, biodiversity)



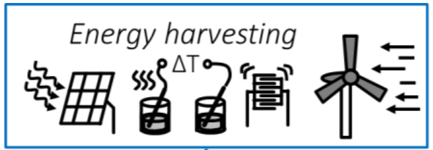
- ✓ Limited risk of detour
- ✓ Indirect ecological benefit
- Technological challenge: low absolute direct footprint

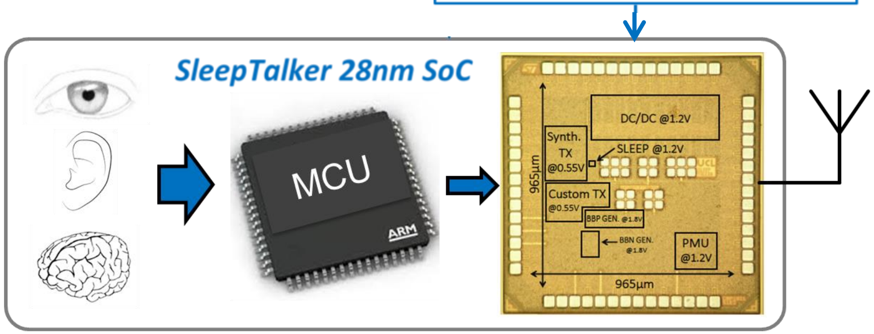
[P. Maistriaux, D. Bol et al, "Modeling the Carbon Footprint of Battery-Powered IoT Sensor Nodes for Environmental-Monitoring Applications », IoT, 2022]

Example D: wireless communications

Before: UWB radio chips for batteryless IoT smart sensors

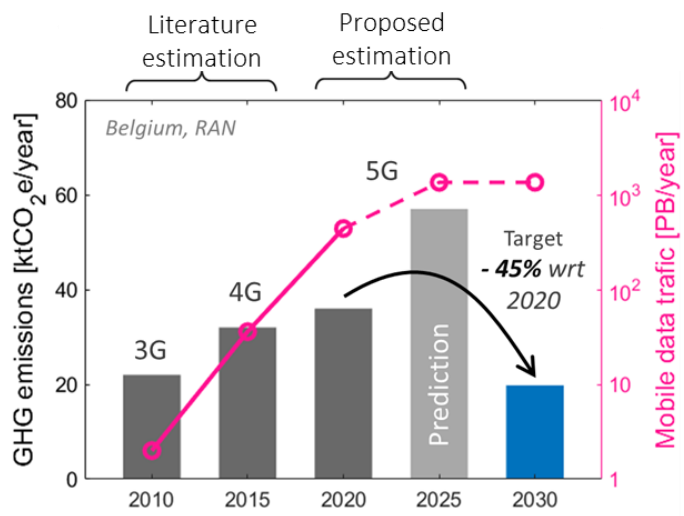
[de Streel, Symp. VLSI, 2017]
[de Streel, JSSC, 2017]
[Schramme, SSCL, 2020]





- ✓ Low *relative* footprint
- × Risk of need creation (futile applications)
- × High risk of rebound effect

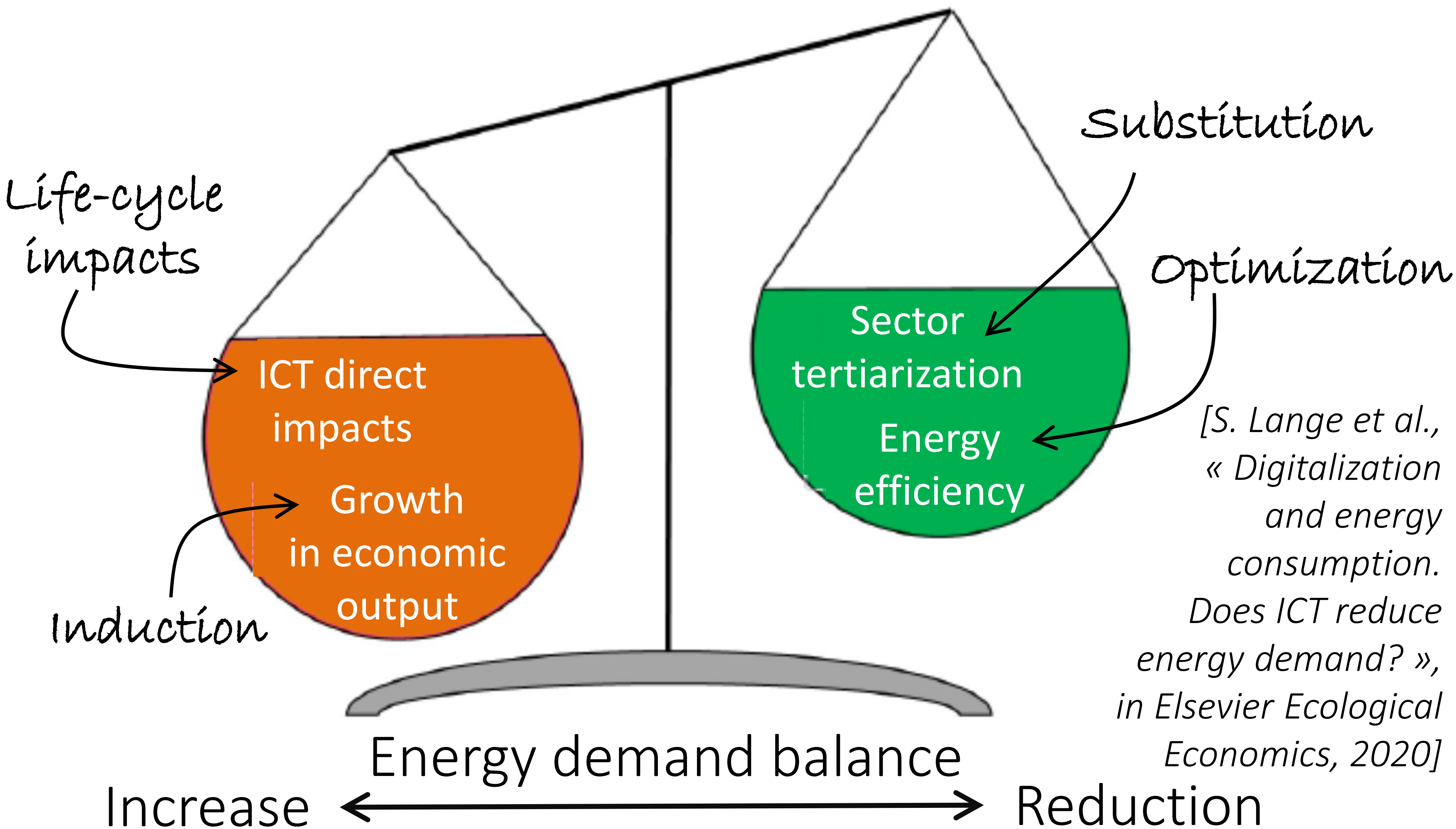
Now: reducing the carbon footprint of mobile Internet access



[L. Golard, J. Louveaux and D. Bol, "Evaluation and projection of 4G and 5G RAN energy footprints: The case of Belgium for 2020–2025", Springer ANTE, 2022]

- ✓ Ecological benefit: reduction of absolute footprint (no rebound)
- ✓ "Need" is already there
- Holistic challenge: manage network saturation

Impacts of digital transformation at the macroeconomic level



[S. Lange et al., « Digitalization and energy consumption. Does ICT reduce energy demand? », in Elsevier Ecological Economics, 2020]

What if re-orienting research is not possible ?

Quitted the following research directions:

× Neuromorphic circuit design –
Applications are speculative with a high potential of detour

× Simultaneous wireless information & power transfer (SWIPT)
At 3-5m range, the carbon footprint over the life-cycle is 10× higher than using coin cell batteries

Post-growth approach = being open to degrowth

Conclusions (1/2)

- Context:
  - the 20th-century lead to the exceedance of several planet boundaries
  - ICTs account for 2-4% of global GHG emissions
- Fact #1: ICT research and innovation are driven by empirical efficiency improvement laws (e.g. Moore's law)
- Fact #2: The follow-up of these laws is correlated in time with an increase of the absolute footprint of ICT
- Thesis: causal rebound effect (Jevons' Paradox): the pursuit of efficiency in ICT led to the increase of its environmental footprint through vicious socio-economic dynamics in the growth economy context
- Corollary: Designing energy-efficient chips is useless if we keep on deploying more chips

Conclusions (2/2)

- Hoping to effectively reduce the absolute ecological footprint of humanity to avoid a global collapse, we first have to depart from the blind faith in the automatic benefits of technological progress
→ No innovation for the sake of innovation
- The 21st-century Anthropocene urgently calls for a transition by complementing the pursuit of efficiency with sobriety, restricting R&I to applications with socio-ecological benefit (clearly demonstrated)
- Open (non technological) question:
how could Humanity agree on meaningful applications in a fair, democratic and informed/science-based way ?