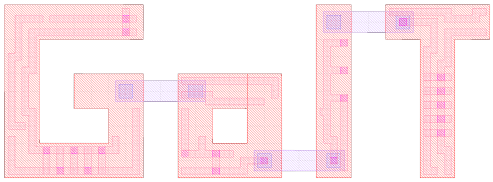

Recommendations and roadmap for the development of open-source silicon in the EU

Free Silicon Foundation (I) ETS

November 3 2023

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Observation: the signed Grant Agreement contains several changes compared to the original submitted proposal. In particular the Free Silicon Foundation (I) ETS is no longer coordinator of the project, the FSI budget was diminished to approximately half of the original amount, and multiple tasks originally assigned to FSI have been assigned to other participants. The updated version of the proposal (Grant Agreement) has not been published.

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2 Executive summary

After a brief introduction which defines the necessary terminology and introduces the political background, in chapter 4 we argue that open-source Electronic Design Automation (EDA) tools and open-source silicon are essential instruments to achieve many of the goals set by the Chips Act. This chapter does not provide any recommendations yet.

In chapter 5 we analyse the "**Design Platform**" foreseen by the Chips Act in the light of the feedback obtained by interrogating multiple European SMEs involved in chip design. **Potential problems were identified** with the foreseen cloud-based infrastructures. These are related with security, privacy, the too large spectrum of tools, forced upgrades, increased control by EDA vendors, and increased risk of discovery of patent infringement. To mitigate these problems **we recommend** to support, besides cloud installations, also ***local* EDA installations**, and **we recommend to support open-source EDA flows** besides the commercial flows.

In chapter 6 we analyse the role of standards and standards-setting bodies in the context of open-source. In particular we highlight how open-source development has needs which are substantially different from the mainstream industrial approach to standardization. We highlight in particular a set of **necessary conditions that, in our experience, standards must fulfil** in order to be adopted by the open-source community.

In chapter 7 we discuss **academia**. We argue that academia can and should play a significant role in the development of open-source EDA tools and open-source silicon. For fostering open-source development in universities **we recommend that the metrics to evaluate academics should include open-source projects** aside to publications, citations, etc. Next, we highlight how there are two classes of academics, which are both essential: *developers* of EDA tools and *users* of EDA tools. Given the near complete disappearance of the former, **we recommend that a new generation of professors is hired to develop open-source EDA tools and to revive the corresponding knowledge in Europe.** In this chapter we finally highlight how people who have not been exposed to open-source solutions often don't appreciate its potential therefore creating a cultural bias. In conclusion, also because of other conflicts of interest, **we recommend to introduce *new* and *independent* personnel in academia**.

In chapter 8 we present an open letter about **ecological sustainability**. The signatories of this letter **recommend**: 1. more sober technology, 2. the "6Rs" (refurbish, reuse, repair, reliability, reduce, recycle) for electronic devices, 3. external and independent auditors for Life Cycle Assessments (LCAs), 4. encouraging world-wide regulations to limit the environmental impact in the ICT sector.

In chapter 9 we discuss **patent threats** and possible upcoming problems for open-source development. Unfortunately **we have no consolidated recommendations yet**.

In chapter 10 we briefly discuss possible **implications of Artificial Intelligence on chip design**. **We warn that** the advent of AI might produce an increased silicon-technology gap between owners of AI and the others. **We recommend to** put in place mechanisms to prevent a further power unbalance between large and small actors. **A possible mechanism consists of guaranteeing a fully open (i.e. down to silicon) development of AI**.

In chapter 11 we discuss the **Cyber Resilience Act (CRA)** and **we recommend that:** 1. the concept of open-silicon is added to the CRA, and 2. open-silicon is recognized as a key ingredient to achieve some of the hardware cybersecurity goals.

In chapter 12 we finally present a **roadmap** for open-source silicon development. First we make a list of open-silicon chips which can be realised immediately or in the near future and highlight their impact. **We then recommend to rapidly finance projects similar (in scope and management) to the DARPA OpenROAD project for open-source EDA development. This is our strongest and most important recommendation**. Next, we list all political handles that policy can operate to foster open-silicon development. Finally we present a **recommended timeline** for the different activities and we conclude.

3 Introduction

3.1 Definition of *open-source silicon*

For "*open-source silicon*" (or "*open-silicon*" in short) we define a silicon chip whose design is open in its *entirety*, from the high-level hardware description, all the way down to the *layout*. Since major Electronic Design Automation (EDA) vendors usually do not allow the publication of any output generated with their tools, an open-source silicon chip must be designed by other means. In practice this implies the use of open-source EDA tools.

3.2 Global open-source EDA landscape

As a consequence of the U.S. export control over cutting-edge EDA tools to China (https://ucigcc.org/wp-content/uploads/2022/12/kleinhans-working-paper_-IGCC-2022-1.pdf), and as a consequence of the high-cost of mainstream EDA tools, multiple Countries worldwide are developing their own proprietary and open-source EDA tools. In China for example there is the open-source tool iEDA/iFlow (https://gitee.com/ieda-iflow/iFlow). Researchers of Countries in Brasil or India have already made significant contributions to existing open-source EDA tools (OpenROAD in particular) (https://ieeexplore.ieee.org/document/9256538) demonstrating the technical capacity of eventually creating their own open-source flows.

The most important and successful effort so far is the U.S. DARPA-funded **OpenROAD project** (https://theopenroadproject.org/). It started in 2018 by answering a specific call of the U.S. government for creating *better* EDA tools than the commercial ones. By leveraging intrinsic advantages of open-source EDA tools over proprietary ones, such as the capacity of running countless parallel instances in parallel (which is impossible using proprietary tools given the unaffordable licence costs) and of quickly adapting the code to the new paradigm, OpenROAD targeted revolutionary concepts like:

1. No-man-in-the-loop: Commercial EDA tools are clumsy, extremely complicated, and require significant human intervention when “compiling” a silicon design. Open-source instead can take advantage of massive parallelization to replace human work through Machine Learning (ML).
2. 24 hour turnout time for RTL-to-layout synthesis, i.e. the time that an EDA tool takes to generate a manufacturable layout of a *digital* design starting from a Register-Transfer Level (RTL) abstraction language like Verilog or VHDL.
3. Overcome the cost barrier of existing EDA tools.

The OpenROAD project has been widely successful and has been used to produce clean layouts all the way down to **12nm nodes** (https://www.youtube.com/watch?v=z-yoZuJx2IE). The project however will unfortunately terminate on December 2023 after the complaint from an EDA company in front of the U.S. government. It appears that the complaint was based on the argument that “*OpenROAD endangers one of the last domains of U.S. supremacy*”.

The OpenROAD project will try to survive the ending of DARPA funding by seeking private funding and donations through the newly born *OpenROAD initiative, a* 501(c)(3) Nonprofit organization (www.openroadinitiative.org).

The OpenROAD project, and the corresponding U.S. calls called IDEA and POSH, have *not* recognized that open-source EDA is an enabler of open-source silicon. The U.S. programs in fact were only targeting the EDA ecosystem alone.

3.3 Power of influence of mainstream EDA tools

Mainstream EDA companies have the power of influencing SMEs, foundries and academia to an extent which can be hardly imagined. Only players of the size of NVIDIA have the power to speak up. The FSI has witnessed the effects personally in academia and through conversations with SMEs.

The power is exerted as follows:

By being an oligopoly, or duopoly, access to mainstream EDA tools are an existential need for SMEs, foundries and university professors. They often receive, after negotiations, very significant discounts over the full licence costs. These discounts make the difference between having access or not to the tools, therefore between success or bankruptcy. None of these entities are in the position to speak up because of the risk of *retaliation* on the licence cost.

Through personal discussions with people involved in the field, we learned that mainstream EDA companies have allegedly utilized extensive legal aggressions over competitors. For example, they have sued companies over patent infringement to lower their market price before acquisition or sent frequent “cease and desist” letters. It is possible that mainstream EDA companies will attack open-source developers in the future, hence it is necessary to put in place early on protection mechanisms as discussed later in section 9.

3.4 How to measure the impact of open-source

Policy makers who have influence over public investments are often concerned whether such investments will ultimately generate novel enterprises and income through tax returns.

In this section we would like to highlight that **open-source development often generates important secondary effects which are not directly measurable by economic metrics, or at least not on a short time scale**. Such secondary effects affect society as a whole and include for example the *efficiency of labour, the quality of products, the level of education of citizens, the efficiency of public services and goods, the respect of fundamental rights such as privacy, and the quality of life in general*. Better education, for example, can lead to an economic return on a longer time scale because it enables solutions otherwise impossible.

As a consequence, we think that Europe should invest in open-source *not uniquely* for creating short-term returns on investment through tax collection. The present document is written with this concept in mind.

3.5 Protection of the privacy of people contacted

This document is written based on several *informal* and *private* discussions with people met as part of GoIT's travelling activity or as part of our network. The name of these people and their institutions/companies is not provided for respecting their privacy. Still, the readers who are interested to verify the validity of certain claims are welcome to contact us and we will ask permission to create a direct link between the reader and the authors of the claim.

4 Chips Act and open source

In this chapter the Chips Act (i.e. the *Proposal for a REGULATION OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL establishing a framework of measures for strengthening Europe's semiconductor ecosystem*) is reviewed from an *open-source* perspective. **The Chips Act sets ambitious goals which would be, in our opinion, difficult if not impossible to achieve without the help of the open-source software and open-source silicon**.

These individual goals are described in separate paragraphs below together with their relationship with open-source.

4.1 Increasing competitiveness of the semiconductor ecosystem

The Chips Act aims at, quote, "***increasing competitiveness of the semiconductor ecosystem****, and of industry at large, through innovative products for European citizens*".

In order to create a competitive semiconductor innovation, Electronic Design Automation (EDA) tools shall be flexible enough to adapt to the different technologies and the new chips architectures. For accelerating innovation, diminishing costs and increasing independence from external actors it is clear the innovation of EDA tools cannot be outsourced to two or three companies alone. **A public and open-source approach instead can enable a fast and cooperative creation of the tools and knowledge necessary to innovate in fields which are so far marginal, like analog**

neural networks or neuromorphic computing, but which carry a large potential on the future. Open-source tools and Process Design Kits (PDKs) can further lower the entry barriers for SMEs to design novel chips similarly to the way that, in the historical competition between Microsoft and GNU/Linux, the inexpensive (usually gratis) availability of free (libre) and open-source software enabled a far richer, far more complex and far more valuable ecosystem of software solutions. As the entry barriers are lowered, fast prototyping and small volume production of silicon chips become more accessible.

Moreover, if Europe embraces quickly the open-source silicon paradigm it can profit from the first-mover advantage by attracting talented open-source developers and by steering the ecosystem. We consider the example set by the foundry IHP (Germany) (https://github.com/IHP-GmbH/IHP-Open-PDK) with the support of the German Federal Ministry of Education and Research (BMBF, https://www.ihp-microelectronics.com/events-1/detail/openpdk-opentooling-and-open-source-design-an-initiative-to-push-development) a blueprint which should be replicated in other Member States, and most importantly in the case of publicly-funded European foundries.

4.2 Open-source foundry and open-source PDK

The Chips Act foresees the development (to be possibly carried out by IMEC) of an advanced technology node co-funded by public money. Given the public interest and the public economic participation, we advise considering, *after a proper and in-depth study*, whether the foundry shall develop, eventually in parallel with its traditional proprietary counterpart, an *open-source* Process Design Kit (PDK). While we acknowledge that fabrication costs in advanced nodes is far larger than in mature nodes mandating the use of well-established, i.e. proprietary, EDA flows at least for the final sign-off, an open-source PDK for advanced nodes would bring the following benefits:

1. It serves to produce a PDK with less errors thanks to public scrutiny and community development (see also below).
2. It enables to develop open-source EDA *tools* capable of targeting more advanced nodes than today (notice that OpenROAD is already capable of synthesizing manufacturable layouts in 12nm nodes).
3. The design in advanced nodes may require the definition of new standards or languages (e.g. for defining new Design Rules which exist only in advanced nodes). It is important that such new standards or languages are developed under a public rather than proprietary licence such as to be usable by the open-source community.

As discussed during the concluding session of the Free Silicon Conference 2023 (https://peertube.f-si.org/videos/watch/087a7e62-c067-473d-957c-57fd9ce85245), there is a clear consensus among the participants that **a public and transparent open-source PDK *development* will likely lead to a PDK with *superior* quality** when compared to the closed/proprietary counterpart. It is well-known, in fact, among people skilled in the art that PDK development is difficult even for the foundries and low-quality PDKs are frequent. Moreover, **proprietary PDKs have been shown to contain trivial errors** which would most likely not have survived a public scrutiny, see for example Tim Edwards at FSiC2022 (https://wiki.f-si.org/index.php/FSiC2022#Mixed-signal.2Fanalog_design).

4.3 Education and know-how

The Chips Act acknowledges the *acute skill shortage* in Europe. At present, the relatively few European universities which offer a chip design education or, even more rarely, a chip design experience accompanied by fab-less fabrication and in-house testing, are largely leveraging the services offered by Europractice, namely the discounted access to *mainstream* EDA tools, the access to Multi-Project Wafer (MPW) runs and to foundry PDKs. Yet, as testified by direct experience and by the feedback received while visiting EU universities under the GoIT grant, **many students are discouraged from starting a career in chip design by the unfriendliness of mainstream EDA tools** (Cadence and Synopsys in particular) **and by the legal burden involved** (students are usually required to sign several contracts or NDAs with their own universities before the lectures). As a consequence, students are unable to utilize design software at home or on their own machines, and are often kept separated from important technological details which are obfuscated or even encrypted. The education flow set by Europractice, moreover, locks students in the proprietary settings of mainstream EDA vendors, discouraging some students even further.

Open-source software and open-source hardware carry the enormous potential of transforming chip-design into an attractive or “cool” field of research and development therefore attracting, rather than scaring, the most talented students; of lowering the legal burdens for education; and of giving access to algorithms (e.g. of place-and-route tools) and technological details (e.g. material properties) which are today kept secret from the most, but which are essential for innovation.

The potential of academic chip-design courses based on open-source have already been tested with large success in a few pioneering experiments, for example:

1. Prof. Axel Jantsch at the Systems on Chip laboratory of TU Wien utilizes the open-source RTL synthesis tool Yosys (https://github.com/YosysHQ/yosys) and the open-source place-and-route tools Nextpnr (https://github.com/YosysHQ/nextpnr) in his classrooms. According to a discussion with Prof. Axel performed under the GoIT umbrella, Prof. Axel praised the use of such open-source tools not only to save costs on the licence fees (the fee paid to Europractice is certainly cheaper than the full licence costs, but still significant for an academic budget), but also, and most importantly, because it is easier for students to understand details and algorithms and explore new ideas. As a side-note, the creator of Yosys (which is used even within OpenROAD), Claire Wolf, was a student of Prof. Axel.
2. Prof. Harald Pretl, head of the Institute for integrated circuits at the Johannes Kepler University (JKU) Linz (https://iic.jku.at/team/) has created a novel university lecture where students can design an integrated circuit entirely based on an open-source flow. He has published the entire software suite on a git repository (https://github.com/iic-jku/iic-osic-tools) which is becoming very popular. Prof. Pretl has also performed pioneering work in publishing open-source silicon IP blocks, namely design components open in their entirety down to the *silicon layout*. His work has been announced at the Free Silicon Conference 2023 in July 2023 (https://wiki.f-si.org/index.php/FSiC2023#IP_blocks).

Other examples include:

1. Dan Fritchman at UC Berkeley (one of the pioneering universities in open-source EDA creating for example the Berkeley SPICE electronic circuit simulator later integrated in

most commercial EDA flows), see for example his talk at FSiC2023 (https://wiki.f-si.org/index.php/FSiC2023#Back-end_design_tools_2),

2. Prof. Boris Murmann at Stanford university, see fore example his paper “Democratizing IC Design” (https://ieeexplore.ieee.org/iel7/4563670/9620728/09621274.pdf)
3. Prof. Priyanka Raina at Stanford university teaching VLSI classes using open-source SkyWater 130nm PDK (https://priyanka-raina.github.io/ee272b-spring2021/)
4. Mehdi Saligane at the University of Michigan (https://ece.engin.umich.edu/stories/open-source-hardware-a-growing-movement-to-democratize-ic-design)

Open-source software and open-source hardware enable moreover not only universities but also companies to offer education programs together with simple and cheap access to silicon fabrication. This has been shown already by the “Zero to ASIC course” (https://www.zerotoasiccourse.com/) and by the “Tiny Tapeout” platform (https://tinytapeout.com/) by Matt Venn.

4.3.1 Address skill shortage by creating novel opportunities

In Europe there are multiple design houses which are simple subcontractors for foreign tech giants such as Apple or NVIDIA. These European design houses probably hired some of the most skilled and brilliant EU chip designers, but they do not contribute to the goals of the Chips Act. **Open-source design tools and open-source technologies (PDKs) allow teaching basic principles rather than specific flows**. As a consequence, **a new generation of engineers may emerge** who will be capable of solving larger challenges rather than just fitting into the tech giant ecosystem.

4.4 Access to design tools, services, expertise and know-how

In Article 8, the Chips Act aims at:

(a) *providing access to **design services** and **design tools** [...] as well as to the pilot lines*

(b) *providing the necessary **knowhow, expertise and skills** to the stakeholders*

(c) *ensure access to **expertise, know-how and services** [...] to build skills and competence capacities*

(d) *facilitating the **transfer of expertise and knowhow** between Member States*

(e) *developing and managing specific **training actions on semiconductor technologies** to support the development of the **talent pool** in the Union.*

These goals are related to open-source as follows:

(a) providing access to ***design services*** and ***design tools*** is clearly facilitated when such access is not subjected to legal burdens like contract negotiations or Non-Disclosure Agreements (NDA), and is not subjected to the payment of outrageously expensive software licence fees. Free (as in freedom) and Open-Source (FOS) EDA design tools, instead, comes with no legal burdens and comes usually at no cost.

(b) and (c) ***Know-how, expertise and skills*** are all conveyed throughout proper education. As already discussed in section 4.3, education can strongly benefit from open-source software and

open-source silicon. ***Access to services***, like the design tools or to technology details, are more easily granted when they are not subjected to arbitrary negotiation arguments from EDA vendors (as it is today the case) or when they are not subjected to legal burdens. Here again, open-source can simplify dramatically the situation and improve accessibility to services.

(d) ***training actions on semiconductor technologies*** *to support the development of the* ***talent pool*** can benefit from the advantages of open-source education as already described in section 4.3. Moreover, talented students can more easily retained when training is based on transparent and accessible open-source software, as described in the examples in section 4.3.

Finally, even if there is no mention of it in the Chips Act, we would like to highlight that the ***community*** plays an indispensable role in open-source development in general. This has no equivalent in proprietary settings. The community, in fact, can replace (at least partially) the online support system, provides feedback, reference designs and new features. It is common to see new features included in existing tools "on demand" within a few days. The role of the community should therefore be acknowledged and leveraged to achieve the Chips Act goals listed above.

4.5 Independence from extraterritorial obligations of third countries

Article 11 of the Chips Act specifies that the "*Open EU foundries*" shall, quote: "*guarantee* ***not to be subject to the extraterritorial application*** *of public service* ***obligations*** *of* ***third countries*** *in a way that may undermine the undertaking's ability to comply with the obligations set out in Article 21(1) and commits to inform the Commission when such obligation arises*".

Article 11 therefore excludes the use of foreign EDA tools Cadence and Synopsys which are known to be subjected to embargoes towards Countries whenever these are ranked hostile to the U.S. or as a national security risk. China is a prominent example, followed by the more recent case of Russia as a consequence of Ukraine's invasion (https://www.bloomberg.com/news/newsletters/2022-03-01/u-s-sanctions-on-russia-show-its-global-chip-domination). As we have learned from direct a discussion with a Russian citizen who participated at the Free Silicon Conference 2023, Cadence offices have been shut down in Moscow as a consequence of the U.S. embargo.

The effect of an embargo on mainstream EDA tools would have furthermore **far-reaching and catastrophic effects** over the resilience ambitions of the Chips Act. A large part of the chip-design ecosystem is embedded or linked in subtle ways to those EDA companies in forms that go beyond the simple software licence terms. For example, the **Process Design Kit (PDK)** of silicon foundries are almost always written using **proprietary file formats** compatible only with such EDA tools, or written in a form compatible only with them. An embargo on EDA tools would not only require to redevelop the design tools, but to rewrite the PDK of most foundries, even those built on EU soil and with EU know-how.

4.5.1 Different interpretations about the "independence by extraterritorial obligations"

While interviewing multiple people involved in policy making, we realized that there are multiple incompatible interpretations about this section of the Chips Act. Here are some of them:

1. The danger that EU will fall under US embargo is considered small. There is a much higher risk that companies like Cadence and Synopsys will be purchased by other global actors hostile to the EU.

2. It is unlikely that Cadence and Synopsys will be sold to other global actors because the US has the capacity to block the acquisition of strategic companies

Recent history however has shown how Mentor Graphics, a formerly US-based electronic design automation (EDA) multinational corporation, was acquired by Siemens in 2017. Other examples include the multiple international acquisition of the technology companies (see Oneweb and EUTELSAT) behind Starlink, the US space internet service as summarized in a recent documentary (https://www.arte.tv/en/videos/105563-000-A/satellite-wars/).

4.6 Key Performance Indicators (KPI) in the Chips Act vs. open-source

4.6.1 Design tools development

The Chips Act, lists as "Indicators of performance" of the *Chips for Europe Initiative*, quote, *the number of design tools developed or integrated under the Initiative.*

Rather than developing some proprietary tool which risks to be first publicly funded and then absorbed by the mainstream companies as it happened so many times in the past and more recently with the publicly-funded photonic design suite "PhoeniX Software" purchased in 2018 by Synopsys (https://www.synopsys.com/company/acquisitions.html), we recommend that publicly funded tools are published with a forever-open licence (i.e. copyleft like GPLv3) rather than with a temporarily-open licence (i.e. permissive like MIT, BSD or Apache).

4.6.2 Increasing the number of users getting access to design capabilities

The Chips Act lists as another "Indicator of performance, quote, "*The number of users or user communities getting access to design capacities and pilot lines under the Initiative*".

Again, this speaks in favour of open-source EDA tools and open-source silicon IP blocks given the total lack of entry barriers as compared to the high legal and economic barriers of the proprietary counterparts. The potential of this approach is demonstrated even commercially by the "Tiny Tapeout" platform (https://tinytapeout.com) by Matt Venn and by the "ChipIgnite" offer Program" by Efabless (https://efabless.com/).

4.6.3 Durability, repairability, upgradability, maintenance and reuse

On page 8, the Chips Act states: "*The proposal is in line with the Circular Economy Action Plan 36 , which identifies electronics and ICT as a key value chain and announces a Circular Electronics Initiative to encompass "regulatory measures for electronics and ICT including mobile phones, tablets and laptops under the Ecodesign Directive so that devices are designed for energy efficiency and* ***durability, repairability, upgradability, maintenance, reuse*** *and recycling*".

Since the capacity of users to repair, upgrade, maintain and reuse a device critically depends from the amount and quality of the documentation available on their devices and chips, open-source hardware and open-source silicon chips are clearly an enabler and arguably even a necessary condition for achieving this goal of the Chips Act, see also section 8. For an example see the case of Fairphone 2 whose end-of-life was caused by Qualcomm ending the support for its "Snapdragon 801 SoC" contained in the phone (https://arstechnica.com/gadgets/2023/01/the-fairphone-2-will-hit-end-of-life-after-7-years-of-updates/).

5 The Chips Act Design Platform

The Chips Act foresees the creation of a ***virtual*** *design environment* , where the term "virtual" is interpreted as "cloud-based" and not as "run on a computer".

5.1 Critical review of the "*Recommendations and roadmap for a Design Platform in the context of the European Chips Act*"

In the following we review the document prepared by the "Design Platform Working Group" nominated by the EC entitled "*Recommendations and roadmap for a Design Platform in the context of the European Chips Act*" of June 2023.

The comments below are based on FSI's experience and informal discussions between the FSI and multiple European SMEs which were contacted for this purpose. These SMEs were given in advance a copy of the "*Recommendations and roadmap for a Design Platform in the context of the European Chips Act*" and could develop therefore an educated opinion.

Most contacted companies said that they would strongly avoid using a cloud-based platform. We are aware that the Design Platform mainly targets entry-level companies such as startups stemming from academia, and not established SMEs like those we contacted. Still, we think that the arguments against a cloud-based system may help understanding possible issues and we propose possible mitigations.

5.1.1 Common arguments of SME for not using a cloud-based infrastructure

1. **Security and privacy**. Some companies have strict confidentiality requirements either for the customers they work for, or for themselves for protecting their own IP. It is not rare that an SME runs their entire design infrastructure on a dedicated subnet which is completely cut off from the internet. A cloud-based approach, would very hardly manage to offer sufficient guarantees for such companies. Any business requiring such levels of security and privacy would be cut-off from the foreseen cloud-based design infrastructure. **Proposed mitigation**: create a centralized system only where it is truly beneficial, such as for the management of legal documents (software licences, access to standard IP blocks like standard cell libraries, foundry PDKs, etc.), for the maintenance of installation scripts for the multitude of different EDA/PDK combinations, and allow everyone who intends to do so to install a *local* copy of the software in their *own IT infrastructure*.
2. **Difficulty of maintaining the too large spectrum of different needs**. There is a very large number of different EDA tools, of different PDKs, and different operating systems. The

number of combinations of these three is enormous. Different operating systems must be taken into account because some companies, for example, have developed their custom tools which run only on specific operating systems (like the CentOS6 which has already reached official end-of-life but which continues to be utilized on isolated networks).
Proposed mitigation: as above, allow and facilitate the SMEs to have local installations and to customize their own needs.

3. **Forced upgrades**. Given the practical difficulty of supporting the wide spectrum of possible needs, a centralized infrastructure will probably cause that designers will be invited (more or less willingly) to utilize some specific tool versions. This scenario appeared very critical during some interviews.

4. **Accessibility (who is the *root* user of the server?)**. In the chip design industry it is frequent to have sharp deadlines and high economic penalties for missing them. Companies generally require that somebody can quickly work and fix on the (frequent) problems that a design involves. Modifying tools, upgrading libraries, accessing corrupted data generally requires high access privileges on the server which hosts the tools (namely being a "*superuser*" or "*root*" user), if not even physical access to the hardware. A centrally-managed cloud design infrastructure is hardly compatible with these needs.

5. **Increased control by EDA vendors**. A centralized system running mainstream EDA tools encourages mainstream EDA vendors to offer their own products rather than alternative open-source or other proprietary solutions. Given the past history about non transparent licence discount policies (unfortunately we have no written evidence but an overwhelming amount of oral testimonies), this fear is very common.
Proposed mitigation: offer open-source EDA tools on the cloud alongside proprietary tools. The installation scripts of such tools should be public such that everybody could opt to make a *local* installation.

6. **Increased risk of discovery of patent infringement.** Discovering that a hardware patent has been violated (eventually in good faith) in a closed-source proprietary silicon chip is technically very difficult. Instead, hosting and synthesising a chip design on a cloud to which third parties may have access to, could increase the risk of discovering patent infringement.

6 The role of standardization and of standards-setting bodies

In the open-source domain, standards are fundamentally different from the historical industrial domain. We think that a standard must fulfil the following necessary (not necessarily sufficient) conditions in order to have reasonable chances to be useful or adopted by the open-source community:

1. **The definition of a standard must be easily accessible to everybody at no cost**. This is in contrast with the usual business model of standards-setting organizations putting the definition of a standard behind expensive paywalls or subscription fees.

2. **The process of defining a standard must occur over a public and online process** in order to be transparent, to be freely accessible and to guarantee accountability. There should be no room for hidden negotiations or bias due to economic interests. This can be achieved, for example, but utilizing mailing lists as done most of the time by the Internet Engineering Task Force (IETF) or through digital platforms which are familiar to open-source software development, such as Codeberg or GitHub. An example of such a development is used for the standard DIN-SPEC 3105 (https://gitlab.com/OSEGermany/OHS-3105).
3. **Mechanisms shall be put in place for facilitating merging rather forking standards**. The goal is to decrease rather than increase the number of standards. We think that the RFC (request for comments) approach used, e.g. by the IETF is an effective mechanism to achieve this goal by fostering alignment. The RFC system moreover is relatively immune to the bias from interest groups because everyone considered an expert can make a proposal without particular weight in some committee and the acceptance is a matter of technical quality rather than of business benefit.
4. The adoption of a standard should not be driven by the authority of a standards-setting body, but by the quality of a standard. For *hardware* standards, e.g. WiFi standards, the process of converging to a standard of sufficient quality may require multiple and expensive fabrication iterations. Open-source development may effectively cut the development costs. Enterprises (including SMEs) might be incentivized to produce open-source hardware reference implementations (IP blocks) for example by a competitive public funding scheme.
5. Given the fast pace which is typical in open-source development, a standard should be easily upgradable.
6. Whenever possible, **the standard should include a *software reference implementation* or consist uniquely of a reference implementation (properly documented)**. This should be commonly achievable in the context of open-source silicon. For example, the definition of a hardware language like Verilog, should not come only in the form of a .pdf file, but also in the form of a software *reference implementation* which can read, write and interpret files written in Verilog.

6.1 The ambiguous definition of the term “open standard”

As summarized on Wikipedia there is currently no general consensus on the definition of “open-standard” (en.wikipedia.org/wiki/Open_standard#Specific_definitions_of_an_open_standard). Multiple entities, such as the Word Wide Web Consortium (W3C), the Free Software Foundation Europe (FSFE) and multiple governments have provided their own. We will therefore avoid using this term here.

6.2 Standardization of language formats.

The commercial Electronic Design Automation industry currently functions thanks to a number of *de facto or formal standard* languages which define how all the software tools involved in the design process interface with each others. Examples are LEF/DEF, DRC rules, transistor models (BSIM, HSPICE, Xyce-compatible, ngspice-compatible, etc.), layouts (GDSII, OASIS), and

hardware description languages (Verilog, SystemVerilog, VHDL and their subsets). Some of these languages, such as Verilog, have been standardized by the IEEE but the full specification of the standard is so large and complex leading to the creation of subsets of such languages. We currently don't have a solution to improve the current situation, but we would like to show with the concrete example of GDSII described in the following section, how open-source has facilitated a wide adoption of a language.

6.2.1 The example set by the *GDSII* file format for chip design, a format out of anybody's control

Short definition of layout file: Every silicon chip, before being fabricated by a foundry, is represented in the form of a *layout* file. The layout defines the "black or white" areas of the lithographic masks used by the foundry to produce the chip. Since multiple masks are used (e.g. for silicon etching, ion implantation, metal wires, etc.), the layout contains multiple layers, for example one for each mask.

The GDSII file format, together with the OASIS file format, is one of the most common file formats used for layout. This format is so widespread that most chip designers expect that the tools they use are capable of processing GDSII files.

The GDSII file format was initially developed in 1978 by Calma, a computer graphics company based in California. In the same year, Calma was purchased by United Telecommunications Inc. (UTI) based in Missouri. In 1980 UTI sold Calma to General Electrics (GE). In 1988 GE sold the electronic division to Valid Logic System which was finally acquired by Cadence Design Systems in 1991. Cadence claims since the ownership of the GDSII file format.

While the GDSII format was officially part of Cadence Design Systems, it witnessed a **parallel open-source development**. In 1994, in fact, the GDSII file format was for the first time publicly described in the appendix of the well known book by *Steven M. Rubin* entitled "*Computer Aids for VLSI Design*" and freely available on the internet (https://rulabinsky.com/cavd/). This book highlights the incredible simplicity of the GDSII file format which was an inspiration for many open-source GDSII software implementations including KLayout.org (whose author is a co-founder of the FSI). Since no (known) legal action was taken by the owner of the GDSII file format, the format became to some extent an "open format" (note: we are aware that the definition of open format is loose). In its original definition, the GDSII file format defined the maximum number of layers to be 256 (partly because of the limited capacity of computers back then). However, while Cadence Design System still uses the same restriction in its GDSII definition, most of the software implementations of GDSII format support nowadays a maximum of 65535 layers.

In conclusion, this example shows that once the format definition has become of public domain (thanks to the book of Steven M. Rubin in this case), it has in practice lost any control from the "owner" of the format. Moreover, the simplicity of the format, once revealed to the public, encouraged many people to write their own implementation, transforming the GDSII into a widely adopted *de facto standard.*

7 Academia

7.1 Rewarding open-source activities in academia

With a nearly unanimous consensus, all professors, researchers and students met as part of the GoIT project (the project foresees visiting most European universities involved in chip design) agree that if the EU wants to foster open-source innovation in academia, then **the metrics to evaluate academics should change and should include open-source projects** aside to publications, citations, h-factors, etc. Students and researchers who seek an academic career by being promoted to a professorship or leadership position, or who seek grants from the EU, national and regional institutions, currently have no incentive to contribute to open-source projects because such projects absolutely don't matter (with very rare exception) when evaluating their Curriculum Vitae and the impact of their research. In some Countries, such as Slovenia and Latvia, the ministry in charge defines precisely the criteria of selection of academic personnel. Such metrics says that only peer-reviewed journals with a certain impact factor can be used for the evaluation, and open-source projects are completely ignored.

7.2 The near total disappearance of EDA know-how

Despite Europe has historically played a relevant role in developing core know-how about algorithms used in mainstream EDA tools, such knowledge has today almost completely disappeared from European universities. **If progress is to be made in *improving* (not using) open-source EDA tools, it is essential that this knowledge is revived**. Most university professors in the field however are mostly *using* rather than *developing* EDA tools, and it is therefore unlikely that they can perform this task. Again, we think that a new generation of professors should be hired to fill this gap.

7.3 Lack of open-source culture and conflicts-of-interest in academia

From previous experience and while visiting universities across EU, we noticed that **professors and researchers who have not been exposed to the open-source culture have difficulties to understand concepts of open-source and its potential**. On the contrary, people who are familiar with the open-source world are generally enthusiastic about the idea of open-source silicon, strongly believe in its necessity from a security and democratisation perspective and would be able to engage immediately in case that funding and academic recognition was available.

Some prominent European professors moreover are tightly linked with the major EDA vendors, creating an evident conflict of interest and potentially biased views.

Recommendation: We recommend therefore to introduce *new* and *independent* personnel into academia. As a possible mechanism to achieve this goal, we suggest the EC to create specific calls targeting *open-source EDA and hardware* development. Such calls could be inspired by the ERC StG format where the winners are not bound to a single institute but generally welcomed in any university. In this way they can contribute to shift the decision making of the academic council and steer research and education towards a more open-source-oriented approach.

7.4 The skill set for open-source EDA and open-source silicon development

As highlighted in a recent talk (https://www.youtube.com/watch?v=z-yoZuJx2IE), the Principal Investigator of the OpenROAD project, Prof. Andrew Kahng, the ideal person to work on open-source EDA development has, quote, "*good software development skills and the right mindset*". According to Prof. Kahng, it is easier to learn the chip design flow (physical design and EDA understanding) than learning software development skills. This experience matches our own. Unfortunately in most universities the two skill sets are taught in different departments: electrical engineering and computer science respectively. To accelerate the evolution of academic curricula, we suggest, as above, that ***new* professors should be properly selected and hired**.

8 Ecological sustainability

At the past Free Silicon Conference (FSiC2023) Sorbonne University and the FSI have organized a session about sustainability. Most speakers address the ecological-sustainability (as opposed to the economical sustainability). Following the event, a common statement was prepared and published at the following URL:

https://wiki.f-si.org/index.php?title=Recommendations_for_the_EC_on_how_to_reduce_the_environmental_impact_of_the_ICT_sector

For convenience, this statement is copied below:

8.1 Statement

This page contains a number of comments and recommendations for the European Commission on how to reduce the environmental impact of the ICT sector.

This initiative originated during the "Sustainability session" at the Free Silicon Conference 2023 (https://wiki.f-si.org/index.php/FSiC2023 and the views are shared by all the signatories listed at the end of the document.

There is a general consensus in the academic literature that the environmental impact of Information and communications technology (ICT) needs to drastically decrease in the coming years, as for all economic sectors, and that its current trajectory is not sustainable [Freitag21,Pirson23]. The direct environmental impacts of ICT devices notably originate from the various phases of the device life cycle:

1. design and fabrication (e.g. emission of polluting gases as fluorinated compounds for silicon etching, greenhouse gas (GHG) emissions due to electricity consumption)
2. usage (e.g. energy consumption)
3. disposal

The environmental impacts of device design & fabrication, called embodied impacts (e.g. embodied GHG or carbon emissions for the climate change impact), have often been neglected in academic

publications, but play for some type of devices, like the ubiquitous smartphones, the dominant role [Gupta21]. The end-of-life of systems is today dealt with direct landfill in more than 82% of electrical and electronic devices [Forti20]. The GHG emissions of device disposal will most probably rise when system end-of-life will include more recycling to minimize e-waste.

The global race for "better" devices (more capable, more energy efficient, faster, smaller, etc.) has been associated over the entire ICT history with a significant rebound effect (https://en.wikipedia.org/wiki/Rebound_effect_(conservation)) which has caused an overall increase, rather than decrease, of the environmental impact of the ICT sector. Positive indirect effects of the progress of the ICT sector (e.g. less polluting travels thanks to more video conferences) are 1) difficult to quantify exactly because of the mathematical uncertainty on the available data, and 2) counterbalanced by negative indirect effects (e.g. more consumption of goods because of e-shopping). Therefore, the positive indirect effects cannot justify uncontrolled growth in direct GHG emissions of the ICT sector.

Yet we (the signatories below) all agree on the following recommendations:

- technology should become dramatically more sober in a short term. Programmed obsolescence (e.g. of smartphones), creation of futile needs (e.g. ubiquitous video consumption), unnecessary race for sensors-everywhere and ubiquitous data collection (IoT) should be contrasted. We think that the current economical model is disfunctional and should be rediscussed. We welcome the recent regulation (EU) 2023/1670 which guarantees the right-to-repair for smartphones and tablets for at least 7 years after the end of the distribution on the market and we advise that it will be extended to a broader class of devices after carrying out a duly preparatory study in line with the statement of repair.eu at https://repair.eu/news/we-need-the-right-to-repair-to-be-universal/. Drastic reductions of GHG emissions will need to be conducted for all families of electronic products for the Paris climate agreement to be respected, as the current global trajectory is far from the Paris agreement objectives [UN22]. In this context, it is clear that the open-silicon movement can play a role thanks to openness of the documentation and to the accessibility of open-source tools for repurposing or updating devices.
- The modularity of electronic products and their compatibility between vendors should increase for minimizing the disposal of yet-perfectly-functional devices or components. We think, for example, at computer components, embedded systems and power components like batteries and inverters. New businesses for refurbishing and reusing components shall emerge and be supported by European Union. More generally, components shall be used until reaching a physical reliability limit, employing the six methods defined in the EU EECONE project for acting on electronics carbon impact: refurbish, reuse, repair, increase reliability, reduce, recycle (6Rs https://www.eecone.com/eecone/home/). For this purpose also, open-silicon is key to achieve large scale 6Rs.
- Innovations targeting lower GHG emissions, lower waste and increased fairness will succeed only if external, independent auditors make the Life Cycle Assessments (LCA)s (like Fraunhofer for Fairphone 4 [Sanchez22] and Thinkstep AG for Dell R740 [Busa19]) and conclude on sufficient improvement of KPIs from one product to the next.

- Europe alone can set high standards and become an example to be blueprinted globally. Yet, the market size of EU is limited and EU should encourage the creation of world-wide regulations to limit the environmental impact in the ICT sector. For example, a) imposing product-level GHG emissions and waste disclosure with advanced information on the whole value chain (including Scope 3 and location-based Scope 2), as a complement to company-level carbon disclosure defined by the Greenhouse Gas Protocol [GHG04] and the European Sustainability Reporting Standards , and b) banning from the EU market products with too low environmental or fairness standards.

These actions can define a novel EU-initiated family of ICT systems and the corresponding design methods that will pave the way for deploying sustainable technologies on a global scale.

Signatories:

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9 Patent threats

We foresee that major EDA companies may attack open-source EDA developers as soon as open-source tools or open-source designs become sufficiently impactful. EDA companies are known for aggressive litigations, see 3.3. To prevent such threats from happening and avoid patent trolling, it is advisable to foster the early creation of defence mechanisms. We have not consolidated recommendations on this topic yet. For additional literature we would like to point to the “End Software Patents” wiki (https://wiki.endsoftwarepatents.org), and the “Patent Commons Project” (https://en.wikipedia.org/wiki/Linux_Foundation#Patent_Commons_Project).

10 Artificial Intelligence and chip design

Artificial Intelligence (AI) has been used since several years by commercial EDA tools, but so far it has mainly replaced or improved tasks which were already performed by a machine (such as place-and-route) with other tasks still performed by a machine. Such techniques involved mainly Machine Learning (ML) techniques.

On May 2023 an article claiming to describe “the world's first wholly-AI-written HDL for tapeout” was published (https://arxiv.org/abs/2305.13243). This work used Large Language Models (LLMs). On August 2023 a second paper made similar claims (https://arxiv.org/abs/2308.10204). While it can be argued whether the use of AI in the first paper was beneficial compared to the canonical human-made design, these papers hint that better generations of AI may replace in the future significant amount of human efforts for designing a chip. **Since better chips lead to better AI, and better AI would then lead to better chips, a positive feedback loop would be created**. As a consequence, those who first develop AI could accumulate over time an even larger advantage over all others.

Recommendation: Put in place mechanisms to prevent a further power unbalance between the large actors and the smaller or public ones. A possible mechanism consists of guaranteeing a fully open development of AI (i.e. down to the silicon level). As an additional resource, compare the recommendations of the Software Heritage at https://www.softwareheritage.org/2023/10/19/swh-statement-on-llm-for-code/ .

11 Cyber Resilience Act (CRA)

As already addressed in the letter sent on July 4 2023 by the Open Forum Europe (OFE) to ITRE Rapporteur & Shadows, co-edited and co-signed among others by the FSI, we are concerned that the concepts of open-hardware and open-silicon have not been addressed in the CRA.

In this section we would like to add that open-source silicon can play a decisive, if not ultimate, role in guaranteeing the security of a large class of silicon chips thanks to the openness and auditability of the design and the verifiability that the fabricated chip matches the layout. We recommend that the current CRA document will be adapted not only in a way that does not obstruct the development of open-silicon, but possibly even fosters it by recognizing open-silicon as a key ingredient to achieve some of the hardware cybersecurity goals.

12 Technical roadmap

In this chapter we finally present a possible roadmap for open-source silicon development. In the first section of this chapter we present a list of concrete examples which are at reach of open-source silicon and put them in the context of their impact. In the second section we present the “political handles” than can be used to achieve these goals. In the last section we give a timeline representation of the proposed activities.

12.1 Devices to target: complexity, impact and timeline

In this section we present a list of silicon devices which in our opinion would be beneficial to develop as open-source silicon chips, starting from the most simple ones which could be fabricated with the available *open-source* EDA tools and PDKs already available, ending with the most complex devices which still require an ecosystem of tools and libraries to be further developed.

12.1.1 Open-silicon Root-of-Trust (RoT)

This objective is the realisation of a silicon design which is sufficiently *secure* and *general* in scope to be adapted to a multitude of scenarios, such as in Hardware Security Modules (HSMs), smartphones, smartgrids, SoCs, etcetera for storing/generating public/private cryptographic key pairs. The fundamental properties of the RoT, like the impossibility to exfiltrate the private keys, should be formally proven (see https://wiki.f-si.org/index.php?title=Physical_security_for_cryptographic_implementations_with_open_hardware) and the design should ideally be kept as simple as possible. Its design should undergo a coordinated and public audit from the best experts in the field. It would replace for example the TrustZone security extension for ARMv8 found for example in the LPC55 microcontrollers of NXP which are currently used by some NitroKey USB dongles and used e.g. for two-factor authentication. The difference is that, by not being a secret black-box, users will have reasonable confidence that it does not contain trivial bugs or malicious features like hardware backdoors. The example set by the ROCA vulnerability (https://en.wikipedia.org/wiki/ROCA_vulnerability) found in the Estonian ID card shows that the “security-by-obscurity” paradigm, which is today mainstream, has limits which can be overcome in an open environment where experts and the public can review and enforce the best-in-class silicon tampering protections.

12.1.2 Open-silicon electronic Identity Card (eID)

This objective is based on the previous: an open-silicon eID would contain an open-silicon root-of-trust, plus some extra analog electronics and minimal digital circuits.

Multiple EU Member States are currently developing their own solutions for identifying citizens through digital means. Some States follow the route of a physical card with a dedicated chips, other follow the route of smartphone “apps” where the security is backed by some Hardware Security Modules (HSMs).

From a technical perspective, the technology contained inside the chip of an eID is at reach of current open-source EDA tools and open-source PDKs. Such chips in fact are very small in size (we estimate a few million gates or less) and can be fabricated in older or mature technology nodes, like

the 130nm node of IHP-Microelectronics GmbH. The chip contains analog blocks for the Near Field Communication (NFC) and a RoT as described above for generating/storing public/private key pairs. While the EU is financing a number of very abstract hardware security projects, there is, as far as we know, no research group who has engaged so far in the proposal of simple and effective open-source eID implementation.

An open-source implementation of an eID would not only be the ultimate way to guarantee proven security, but also a way for the citizens to trust public administrations. Everybody would bring such a chip in the pocket, and even (skilled) teenagers would be able to go home and re-synthesyze the chip that identifies them in front of tax agencies, banks, public administrations, hospitals, or even just cigarette vending machines.

The public scrutiny of such a chip would allow everybody to verify the *data minimization principles* that we think any technology should implement for respecting the fundamental right of privacy. For example, a cigarette vending machine does not need to learn the full name, date of birth, address, tax ID number, etc from someone who just wants to buy cigarettes. It does not even need to know the age of the person, but only if the person is younger or older of a certain age. Similarly, a public administrations or employers don't need to have access to medical information of people, etcetera.

The impact of such an open-source eID would not just be technical, but philosophical too. People like to have control on critical technologies and will not dislike being reassured that their identity is not owned, traded or controlled by some proprietary and questionable companies. Far more people will recognize the democratization potential of open-source creating the necessary **popular consent** for more open-source policies.

An open-source eID will further **facilitate the work of standardization bodies**. Alone in Italy for example there exists three different digital identity cards: the classical ID card, the "tessera sanitaria (SSN)" and the "Carta Nazionale dei Servizi (CNS)" which implement different standards (see ISO/IEC 7816, ISO/IEC 14443 A and B, ISO/IEC JTC 1, ISO/IEC JTC 1/SC 17) and generally require different card readers and different software installed on the PC. As we personally experienced, this creates frustration and mistrust of citizens towards the digitalization efforts of the public administrations. Technically it would have been simple to adhere to a single card and on a single standard, but we suspect that the obscure development process has led to cartels, or other inefficiencies where some private sectors have gained large amount of money profiting from the incompatibility between cards.

An open-source implementation instead would naturally converge towards the most effective solution and towards a single standard.

The EU could create a public and competitive call for creating such a device. We estimate that within two years the winning candidate could propose a full design (including layout) to be published for public scrutiny. After one year of public review such as chip could be mass fabricated and deployed in one or more Member States. **Within five years it could become a Europe-wide reality**.

12.1.3 Arduino-compatible microcontrollers

The design and fabrication of open-source silicon microcontrollers can represent a “pipe-cleaner” for open-source EDA flows and open-source PDKs in view of more complex designs. The simplicity and the availability of such microcontrollers, also thanks to the Arduino platform, could have a strong educational impacts: studying and comprehending such designs could be at reach even for under-18 talented and curious hobbyists. One may begin by designing the smallest and simplest microcontroller found in the Arduino platform, followed by the other Arduino-compatible microcontrollers in order of complexity.

For microcontrollers and their applications usually the “*one size fits all*” rule does not hold. Microcontrollers are found in a large variety of devices and they may run short in time of crisis. An open-source silicon implementation of multiple microcontrollers can mitigate eventual **chip shortages** because an open-source chip design can be quickly adapted to different foundries.

12.1.4 System-on-chip (SoC)

Simple SoCs capable of running small versions of the Linux kernel and with standard peripherals could be the next project in order of complexity to be addressed by open-source silicon. If the SoC is sufficiently powerful, it could be used in widespread educational single-board computers like Raspberry Pi or BeagleBone. This would also enable the general public to build highly secure open-source routers which would in our opinion attract massive attention from the public with the consequent benefits in terms of education and awareness.

Such SoCs, moreover, could find immediate commercial application in open-source laptops such as those built by MNT Research GmbH (https://mntre.com), Such laptops can currently already run open-source microprocessor designs, which are however based on FPGAs (https://mntre.com/media/reform_md/2022-09-29-rkx7-showcase.html). Realizing an open-source processor in real silicon rather than in FPGAs would dramatically increase the clock rate and hence the performance of such devices.

12.1.5 Body implants

While we are not familiar with the legislation of body implants, we think that it is understandable that the general public should have the right of transparency and accessibility on any chip implanted in their bodies, such as pacemakers. No life-critical chip, for example, should depend from proprietary or expensive updates, or on the hope that certain companies do no bankrupt carrying with them, as it happened for the retinal implants by Second Vision (https://spectrum.ieee.org/bionic-eye-obsolete), proprietary communication protocols or other technical details necessary to repair or upgrade such a device. Open-source silicon implementations of such devices would overcome all such problems.

12.1.6 Critical infrastructure

Integrated circuits which are critical to the functioning of a society, such as chips used in power grids, public health, telecommunication, etc. should not contain malicious features implanted by extraterritorial bodies, and should offer reasonable levels of security against unintentional bugs. Unfortunately however, thanks also to the material leaked by Edward Snowden, it is known that

such malicious features have been used in the past (and possibly still are). Open-source implementations could be next goal to target, but more advanced technologies and PDKs should be involved (for example to create routers for the internet backbone). Such devices are not at reach of the open-source ecosystem available so far yet, but can be considered as goals to aim to.

12.2 Open-source EDA development

Open-source EDA tools are *a necessary condition* for open-source silicon because major proprietary EDA vendors usually don't allow to publish any output generated with their tools.

However, existing open-source EDA tools are today far less capable than their proprietary counterparts. For example, significant effort should be invested to create or improve existing timing-drive place-and-route tools, clock tree generators, standard cell generators and verification tools. We think that academia is the correct environment for bootstrapping this development. However, most of the existing groups, by being used to the canonical and proprietary design flows, would not be suited to perform this work. As discussed in 7.3, *new* and *independent* professorships should therefore be hired. To increase the efficiency of the work (e.g. by avoiding work redundancy, by investing sufficient resources in the right areas and by covering all relevant topics) we think that the academic effort should be coordinated. **We recommend therefore to rapidly finance projects similar to the DARPA *OpenROAD* in the U.S.** (https://theopenroadproject.org/). **The OpenROAD project cost about 3 million dollar/year** (which is less than the price of *three* full mainstream EDA licences/year).

12.3 Open-source PDK development

Open-source PDKs are another necessary condition for open-source silicon. The larger the number of open-source PDKs, the better it is for the open-source silicon community. We recommend launching a call for developing additional PDKs which involves both academia and existing foundries leaving such entities arguing about the necessary development costs. See also section 4.2.

12.4 Political handles

In this chapter we summarize the full document and the respective handles that politics can operate to foster open-silicon development:

1. Create public awareness and create public demand, for example by:
    a) mandating the use of open-source silicon in parts of the public sector, such as in critical infrastructure, or for electronic Identity Cards. See 12.1 for specific examples;
    b) improving education of open-source software (e.g. GNU/Linux) and open-source culture from an early age at school, e.g. starting from age 10;
    c) improving technical education of open-source tools and culture in academia by creating new professorships in the area. See section 7 for more details.
2. Finance public research and education (academia)

a) We advice very strongly that EU sets up a program similar to the DARPA **OpenROAD** project in the US (https://theopenroadproject.org/). This project led to the so far most successful open-source EDA design flow, but it still has critical limitations which should be addressed. Such a program should not compete with existing projects, but build upon them. Setting up the framework for a project equivalent to the OpenROAD is not an effort we could afford when writing this roadmap, but we would be glad to coordinate, or help coordinating, such a work.

b) Finance *as soon as possible* new, independent academic professorships. See section 7 for more details.

c) Sponsor low-cost or gratis access to Multi Project Wafer (MPW) tapeout fabrication runs to university/research groups, similarly to the very popular program started by Google end efabless (https://efabless.com/open_shuttle_program).

d) Continue and expand the reach of bureaucracy-free micro-grants to individuals who contribute to open-source development.

3. Finance public-private open-development partnerships (e.g. PDK).

   a) The example set by the German Federal Ministry of Education and Research (BMBF, https://www.ihp-microelectronics.com/events-1/detail/openpdk-opentooling-and-open-source-design-an-initiative-to-push-development) should be replicated and reinforced. See section 4.2 for more details.

4. Foster *economically-sustainable* business models.

   a) A number of open-source silicon or open-source EDA companies already exist on the European continent such as YosysHQ GmbH (www.yosyshq.com) or ChipFlow (https://www.chipflow.io). The number of such companies and their revenue will raise as the demand will raise. However, EU should put in place mechanism to avoid that such companies will follow the same destiny of many other companies in the chip ecosystem, namely of being purchased and disappear into an oligopoly of vendors. We think that a proper licensing scheme based on forever-open licences (copyleft) is key.

5. Legislation: enforce ecological sustainability by enforcing the REUSE principles

   a) As discussed in section 8, open-source is a facilitator to increase the re-usability of devices. Policy shall legislate to make re-usability mandatory at least in certain fields.

12.5 Timeline representation

In this section we present a summarizing timeline of the different activities described in this document. **It is by no means based on in-depth studies but it rather represents our personal and subjective views on a possible trajectory** that would allow to achieve the goals described.

		Year						
Area	**Metrics/Activity**	**1**	**2**	**3**	**4**	**5**	**5-10**	**10+**
Coordination	Launch of a project similar to the OpenROAD project to coordinate European efforts							
Academia	Number of new university professors	20	10	5	1	1	1	1
	Number of novel university courses covering open-source fundamentals	0	20	10	1	1	1	1
	Number of novel lectures about open-source chip design	0	20	10	1	1	1	1
EDA tools	Number of new RIA on open-source tools	10	20	5	5	5	5	5
	Number of new IA on open-source tools	0	5	5	5	5	5	5
	Number of new open-source EDA support/co-development startups (e.g. like Red Hat)	1	2	2	2	2	2	2
Hardware	Open-silicon Root-of-Trust							
	Open-silicon eID							
	Open-silicon Arduino-compatible microcontrollers							
	Open-silicon basic SoCs							
	Open-silicon advanced SoCs							
	Open-silicon critical infrastructure							
Open PDK	130nm BiCMOS IHP Microelectronics GmbH							
	22nm- 90nm node							
	14nm – 22nm node							
	Sub 14nm node							
Legislation	Proposal development for open-silicon regulation							
	Entering in-force of open-silicon regulation							

Table 1: Subjective and tentative estimate of a possible development trajectory. Numbers and timelines must by no means be taken as exact, but just as rough preliminary estimates. ***Legend****: RIA = Research and Innovation Action, IA = Innovation Action.*

13 Conclusions

Policy makers have a big power on influencing the future of open-source development. It is clear that on the short term open-source silicon will play a marginal role, but it can become on the long term a valuable, if not essential, tool to meet not only the goals set by the Chips Act but also to guarantee that silicon technology and all its derivatives are developed in a human-centric, cooperative, innovative and sustainable way. We hope that the EU will acknowledge the role that open-source development can play to reach these goals and will decide to invest strongly and decisively in open-source.