

# **DRC/LVS Development Best Practices**

Learning from GF180 PDK optimization

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#### This is **not** a Lemon!



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### The GF180 DRC/LVS

Project link (efabless fork)

Still active?

https://github.com/efabless/globalfoundries-pdk-libs-gf180mcu\_fd\_pv

- Highlights
  - Nice Python wrapper
  - Large test suite
  - Modular
  - Clean structure
  - References to design manual
- Troubles
  - Performance issue (>10h runtime, >40G memory for medium size layout with 410k stdcells)

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#### Performance Killers

- KLayout bug (garbage collector disabled)
  - Pile-up of memory for intermediate results
- Use of flat mode



- little trust in the other modes?
- Inefficient implementation of certain rules
- After optimization (large test case)
  - speed 10h  $\rightarrow$  1h
  - memory  $40G \rightarrow < 4G$
  - runs on single CPU and consumer hardware

atorkmabrains commented on Nov 30, 2022 @klayoutmatthias That's impressive.





### **Debugging Techniques**

#### Recent features make debugging easier

profile

#### Used at the beginning of a script will print the commands by CPU time and process memory delta

Operation	#	calls
"enclosing" in: sky130A_mr.drc:395	1	
"-" in: sky130A_mr.drc:397	1	
"enclosing" in: sky130A mr.drc:396	1	
"enclosing" in: sky130A mr.drc:388	1	
"&" in: sky130A mr.drc:290	1	
"space" in: sky130A_mr.drc:374	1	
"enclosing" in: sky130A mr.drc:449	1	
"-" in: sky130A_mr.drc:419	1	
"enclosing" in: sky130A mr.drc:384	1	
"width" in: sky130A_mr.drc:368	1	
"enclosing" in: sky130A_mr.drc:421	1	
"enclosing" in: sky130A_mr.drc:418	1	
"-" in: sky130A_mr.drc:289	1	
"space" in: sky130A_mr.drc:435	1	
"width" in: sky130A_mr.drc:428	1	
"interacting" in: sky130A_mr.drc:299	2	
"interacting" in: sky130A_mr.drc:290	1	
"width" in: sky130A_mr.drc:265	1	
"without length" in: sky130A mr.drc:294	1	

Memory returned to system by garbage collector

Time (s)

72.930

70.440

62.270

41.010

38 710

26 070

2 150

19.950 16 750 16.380

15.030

14.380

14.310 13,240

13,190

12.760

12.570

11.260

10.070

Memory (k)

Ω

0

Ω

0

0

Θ

0

0

0

5892

94792

32784

32784

32784

-131136

```
new_target
```

Allows sending intermediate results to a separate layout file for easy inspection





### Choice of Modes

flat (default)

Simple, predictable, single CPU, vanilla implementation

Memory proportional to # objects

Only for small designs or quick checks

#### tiled

Operations work on tiles

Parallelization along tiles, good scaling

Heap allocation for single tiles only

Results / intermediate layers are flat  $\rightarrow$  large memory footprint possible

Range-limited (border specification needed)

**Useful for flat layouts** 

#### deep

Hierarchical processing where possible (local computation done once per cell)

Can be very fast, but also slow (skillful use reqd)

Results / intermediate layers are hierarchical → small memory footprint possible

Scales with "cores <sup>0.5</sup>"

Preferred solution for big hierarchical layouts



# Deep Mode in a Nutshell



\*) OP = "local"

compute(A, B, OP, dist):
 for subject in shapes of A:
 intruders = shapes of B with distance to subject < dist
 results = OP.compute(subject, intruders)
 store results</pre>

Hierarchical treatment

- Compute cell neighborhoods ("contexts")
- Collect intruders per context (→ minimum set of configurations)
- For the results, keep common core inside cell, propagate specific results to parent cells



Deep Mode Best Practices

- Watch for hierarchy degradation
  - Results my be propagated, destroying hierarchy over time

"-" in: sky130A\_mr.drc:294 Polygons (raw): 682248 (flat) 329 (hierarchical) Elapsed: 0.020s Memory: 4391.00M

- Complexity determined by first operand
  - Less shapes, less work
  - The more hierarchical, the better
  - First operand is able to "pull" B shapes down in hierarchy
- Beware of pre-merge
  - Not all operations are "local" and need pre-merge e.g. "interact"
  - Pre-merge will form large polygons potentially higher up in the hierarchy → spoils hierarchical performance

For details see: https://www.klayout.de/drc\_function\_internals.html#drc\_function\_details



#### Klayout is **not** Calibre!





## Klayout is **not** Calibre!

- Immediate execution vs. operation graph
  - Layer == Variable, Value == Layer Geometry
  - Memory allocation == variable lifetime  $\rightarrow$  use "forget" or reset variable
  - Intermediate results allocate memory too (will be cleaned up by GC) d = a - (b & c) - Intermediate result - avoid duplication of expressions
  - No optimization of dead execution branches
    - c = empty & a.interacting(b) Computed even though not needed
  - No selection of input layers based on what is needed
  - No parallelization
  - Pro: allows loops, conditionals and direct per-shape manipulations
  - No hierarchy manipulation
    - Except for variant formation for non-isotropic transformations and grid snap operations



#### Pitfalls we have seen

"drc" function is more generic, but not better than simple equivalents

a.drc(space < 0.2.um) a.space(0.2.um)

Same result, but performance is better with "space"

- Edge "width" != polygon "width"
  - Edge "width" only refers to relative orientation of the edges, but treats edges separately (→ potential long-distance interactions)
  - Polygon "width" is a single-polygon operation on pre-merged polygons

a.edges.width(0.5.um) a.width(0.5)

Similar results, but left side is better with large clusters of polygons while right side is better with large distances

- "+" (join) may be better than "|" (or)
  - "+" simply collects the shapes, "|" merges the shapes → this may give large polygons high up in the hierarchy and eats CPU time
  - For "local" operations, fragmented input is better  $\rightarrow$  use "+"





"+" (join) vs. "|" (or)

poly.or(comp) Gives a single giant polygon over memory area



poly + comp Leaves the original polygons in the hierarchy Executes much faster on

operations not doing pre-merge

12/21



### **Optimization Example I**

#### **Rule**: Max transistor channel length $\leq 20 \ \mu m$

Initial implementation (concept):

```
channel_edges = poly.edges & comp
channel_not_too_wide = channel_edges.width(20.001.um)
error = channel_edges -
```

channel\_edges.interacting(channel\_not\_too\_wide.edges)





#### Analysis





#### **Optimized Version**

Rewriting to polygon width check  $\rightarrow$  range is limited to polygon area



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### **Optimization Example II**

#### **Rule**: NMOS distance to p tap $\leq 20 \mu m$

Initial implementation (concept):

```
nmos = ncomp.outside(nwell)
ptap = pcomp.outside(nwell)
error = nmos.sized(20.um).not_interacting(ptap)
```



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## Rule Implemented Correctly?

nmos = ncomp.outside(nwell) ptap = pcomp.outside(nwell) error = nmos.sized(20.um).not interacting(ptap)



**Effect**: No error reported, as the sized nmos regions are merged and ptap is not outside that merged

nmos.sized(20.um)

nmos.sized(20.um).raw.not\_interacting(ptap) error =

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#### **Optimized + Corrected Version**

Turning around the check optimizes it

Explanation

- ptap has less shapes than nmos
- ptap is localized  $\rightarrow$  pre-merge of "sized" does not spoil the hierachy and is quick.

Effect: "nmos.not\_interacting(...)" has more primary shapes, but has to deal with fewer intruder shapes

```
nmos = ncomp.outside(nwell)
ptap = pcomp.outside(nwell)
error = nmos.not_interacting(ptap.sized(20.um))
```

#### Effect

Execution time drops by a factor 10





# Wrap-up

- Prefer deep mode
- Keep in mind the basic concepts of deep mode
  - First argument should have low complexity
  - Beware of large regions formed by pre-merge
  - Avoid hierarchy degradation
- Use profiling, focus on the greedy ones
- Look at the intermediate results
- Rethink your rule implementation & try alternatives
- LVS: needs hierarchical device recognition layers for schematic / layout correspondence
  - Avoid hierarchy degradation (specifically pre-merge driven)



#### Vision: The Open Source Growth Cycle



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# **Thank you for Listening!**